

# **SIRIUS POWER SUPPLIES: DESCRIPTION, SPECIFICATION AND TESTS**

**5<sup>th</sup> POCPA**

**May 24<sup>th</sup> to 26<sup>th</sup>**

**ELP – Power Electronics Group**

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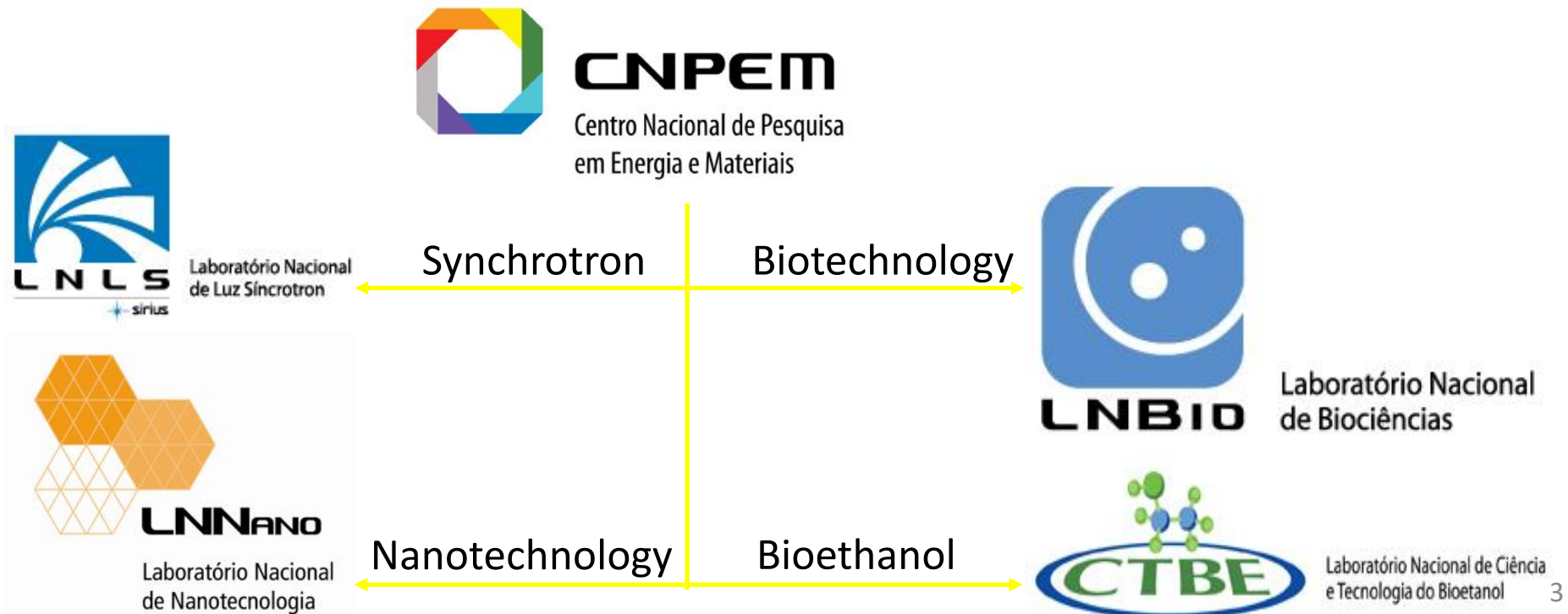
### **2.5 AC POWER SUPPLIES (FAC)**

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## THE CNPEM AND LNLS

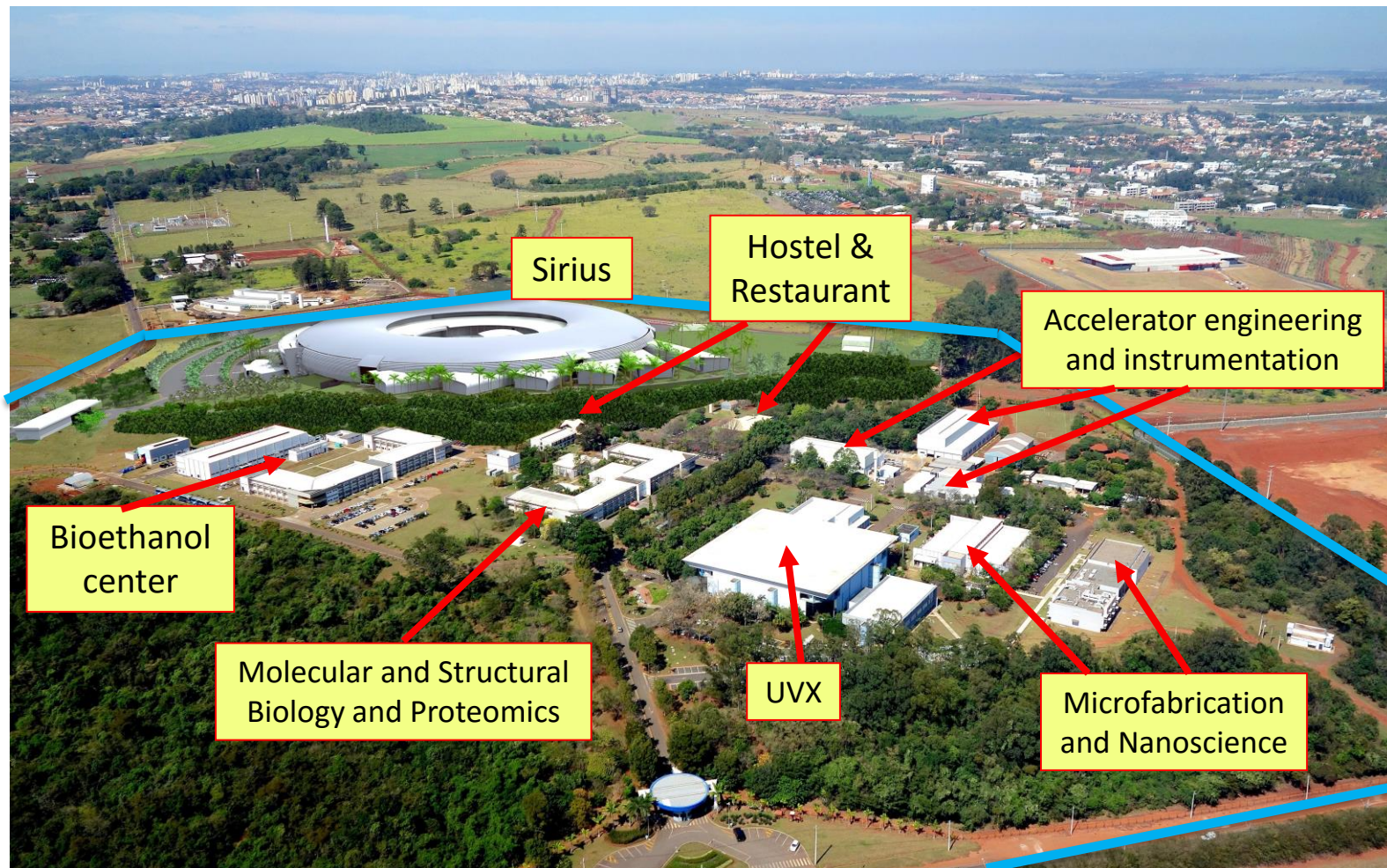
- CNPEM (National Energy and Materials Research Center):
  - Supported by Ministry of Science and Technology of federal government
  - Responsible by 4 National Laboratories: LNLS, LNNano, LNBio, CTBE
- LNLS (Brazilian Synchrotron Light Laboratory):
  - Designed, built and operates the 1<sup>st</sup> Brazilian Synchrotron source (**UVX**)
  - Designing and building **Sirius**, the new Brazilian Synchrotron source



# 1. INTRODUCTION

The LNLS:

- Located in Campinas (São Paulo state)
- Part of CNPEM (National Center of Research in Energy and Materials)





## THE POWER ELECTRONICS GROUP (ELP)

### The Power Electronics Group (ELP):

- 4 Engineers
- 5 Electronic Technicians
- 2 Students



### Responsible For (UVX):

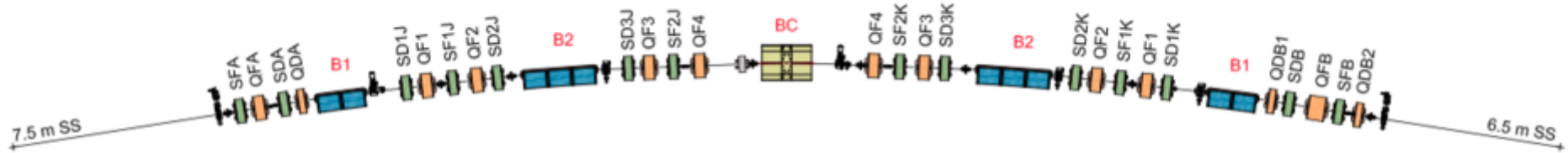
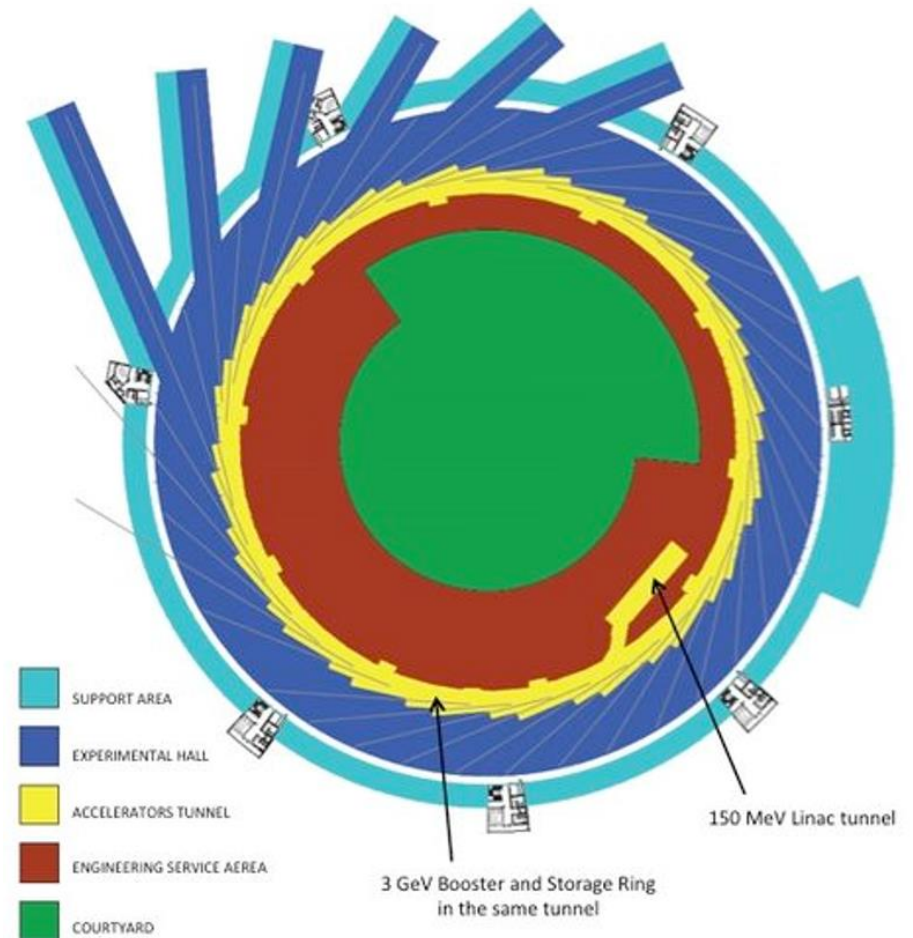
- More than 200 DC Current Source Power Supplies (design, mounting, maintenance):
  - 5 to 500A, 10 to 900V, up to 270kW
- About 20 DC Voltage Power Supplies for valve heaters (design, mounting, maintenance)
- 15 AC Power Supplies for Titanium Sublimation Pump (maintenance)
- About 200 Power Supplies for Ion Pump 6 to 7kV, 3 to 30mA (maintenance)
- Two 80 keV Electron Guns (design, mounting and maintenance)

### Activities in Sirius:

- Design, prototype mounting, tests and coordination of the building of all current source Power Supplies

## THE SIRIUS PROJECT

- **Electron energy:** 3 GeV
- **Circumference:** 518 m
- **Ultra-low emittance:** 280 pm.rad
- **Max. current:** 500 mA
- **RF freq:** 500 MHz
- **13 Beamlines** (first budget)





## THE SIRIUS PROJECT

### Main Dates:

- Jan to Jun/2018: Mounting and installation of subsystems
- Apr/2018: end of building
- Jun to Sep/2018: Commissioning
- Sep/2018: First beam (20mA)



### 2.1 OVERVIEW OF SIRIUS PS

#### STORAGE RING HIGH POWER PS (35 units)

PARAMETER	DIPOLE		QUADRUPOLE MAIN COILS						SEXTUPOLE	
	B1	B2	QFB (Q30)	QFP (Q30)	QFA (Q20)	Qx (Q20)	QDx (Q14)	QDBx (Q14)	S20	S10
Magnets/PS	20	20	20	10	10	40	10	20	20	10
<b>PS Number</b>	<b>2</b>		<b>1</b>	<b>1</b>	<b>1</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>7</b>	<b>14</b>
PS Quadrant Number	1Q		1Q	1Q	1Q	1Q	1Q	1Q	1Q	1Q
Load Inductance [mH]	316		348	174	116	464	63	126	116	58
Load Resistance [mΩ]	1078		1015	570	450	1426	336	548	772	448
<b>Nominal Current [A]</b>	<b>400</b>		<b>150</b>	<b>150</b>	<b>150</b>	<b>150</b>	<b>150</b>	<b>150</b>	<b>150</b>	<b>150</b>
<b>Nominal Voltage [V]</b>	<b>450</b>		<b>225</b>	<b>120</b>	<b>120</b>	<b>225</b>	<b>120</b>	<b>120</b>	<b>120</b>	<b>120</b>
Nominal Power [kW]	180		34	18	18	34	18	18	18	18

#### STORAGE RING LOW POWER PS (830 units)

PARAMETER	STEERING MAGNET					SKEW QUAD		QUAD TRIM COILS		
	SLOW			FAST		Slow	Fast	Q30	Q20	Q10
	Hor.	Vert.	Vert. Ext.	Hor.	Vert.					
<b>PS Number</b>	<b>120</b>	<b>140</b>	<b>20</b>	<b>80</b>	<b>80</b>	<b>80</b>	<b>40</b>	<b>30</b>	<b>170</b>	<b>70</b>
PS Quadrant Number	4Q	4Q	4Q	4Q	4Q	4Q	4Q	4Q	4Q	4Q
Load Inductance [mH]	?	?	6.8	?	?	?	?	10.7	7.2	5.0
Load Resistance [mΩ]	95.6	43.1	74.2	?	?	167	?	332	302	323
<b>Nominal Current [A]</b>	<b>10</b>	<b>10</b>	<b>10</b>	<b>?</b>	<b>?</b>	<b>10</b>	<b>?</b>	<b>10</b>	<b>10</b>	<b>10</b>
<b>Nominal Voltage [V]</b>	<b>10</b>	<b>10</b>	<b>10</b>	<b>?</b>	<b>?</b>	<b>10</b>	<b>?</b>	<b>10</b>	<b>10</b>	<b>10</b>
Nominal Power [kW]	0.1	0.1	0.1	?	?	0.1	?	0.1	0.1	0.1 <sup>8</sup>



### 2.1 OVERVIEW OF SIRIUS PS

#### BOOSTER POWER SUPPLIES (56 units)

PARAMETER	DIPOLE	QUADRUPOLE		SEXTUPOLE		STEERING MAG.	
		QF	QD	SF	SD	Horiz.	Vertic.
Magnets/PS	25	50	25	25	10	1	1
<b>PS Number</b>	<b>2</b>	<b>1</b>	<b>1</b>	<b>1</b>	<b>1</b>	<b>25</b>	<b>25</b>
PS Quadrant Number	4Q	4Q	4Q	4Q	4Q	4Q	4Q
Load Inductance [mH]	90	540	135	50.0	20.0	3.4	3.4
Load Resistance [mΩ]	275	2331	1421	193	156	259	259
<b>Nominal Current [A]</b>	<b>1100</b>	<b>120</b>	<b>30</b>	<b>150</b>	<b>150</b>	<b>10</b>	<b>10</b>
Minimum Current [A]	0	0	0	0	0	0	0
<b>Nominal Voltage [V]</b>	<b>900</b>	<b>600</b>	<b>75</b>	<b>75</b>	<b>75</b>	<b>10</b>	<b>10</b>
Nominal Power [kW]	333	33.6	1.28	4.35	3.50	0.1	0.1
Medium Power <sup>(1)</sup> [kW]	125	12.6	0.48	1.63	1.31	0.013	0.013

<sup>(1)</sup> During injection

### 2.1 OVERVIEW OF SIRIUS PS

#### SUMMARIZING: THREE FAMILIES OF POWER SUPPLIES

- Low Power: 10A/10V, 4-Quadrants, >880 units
    - Steering Magnets, Skew Quadrupoles, Trim Coils, etc.
  - High Power: 150A or 400A,  $8\text{kW} < P_o < 175\text{kW}$ , 1-Quadrant, 35 units
    - Dipoles, Quadrupoles and Sextupoles of Storage Ring
  - AC Power Supplies: 120A (34kW), 150A (5kW) or 1.1kA (333kW), 2Hz, 4-Quadrants, 5 units
    - Booster Dipoles, Quadrupoles and Sextupoles
- 
- ✓ For the LINAC-to-Booster transfer line the electrical specifications of the magnets are still undefined, as well the Power Supplies
  - ✓ For the Booster-to-Ring it was defined that will be used the same dipoles, quadrupoles and steering magnets of Booster
  - ✓ Tests are been made to try use the same hardware of Low Power PS for the fast steering magnets and skew quadrupoles, with few changes

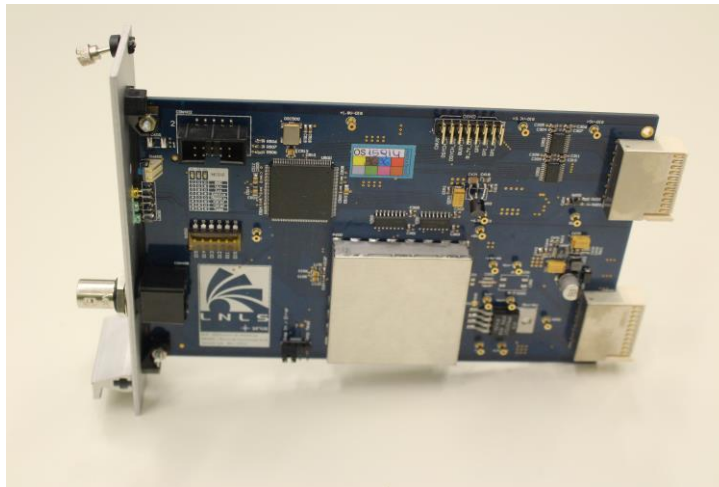
## 2. SIRIUS POWER SUPPLIES

### 2.2 DIGITAL REGULATION SYSTEM (DRS)

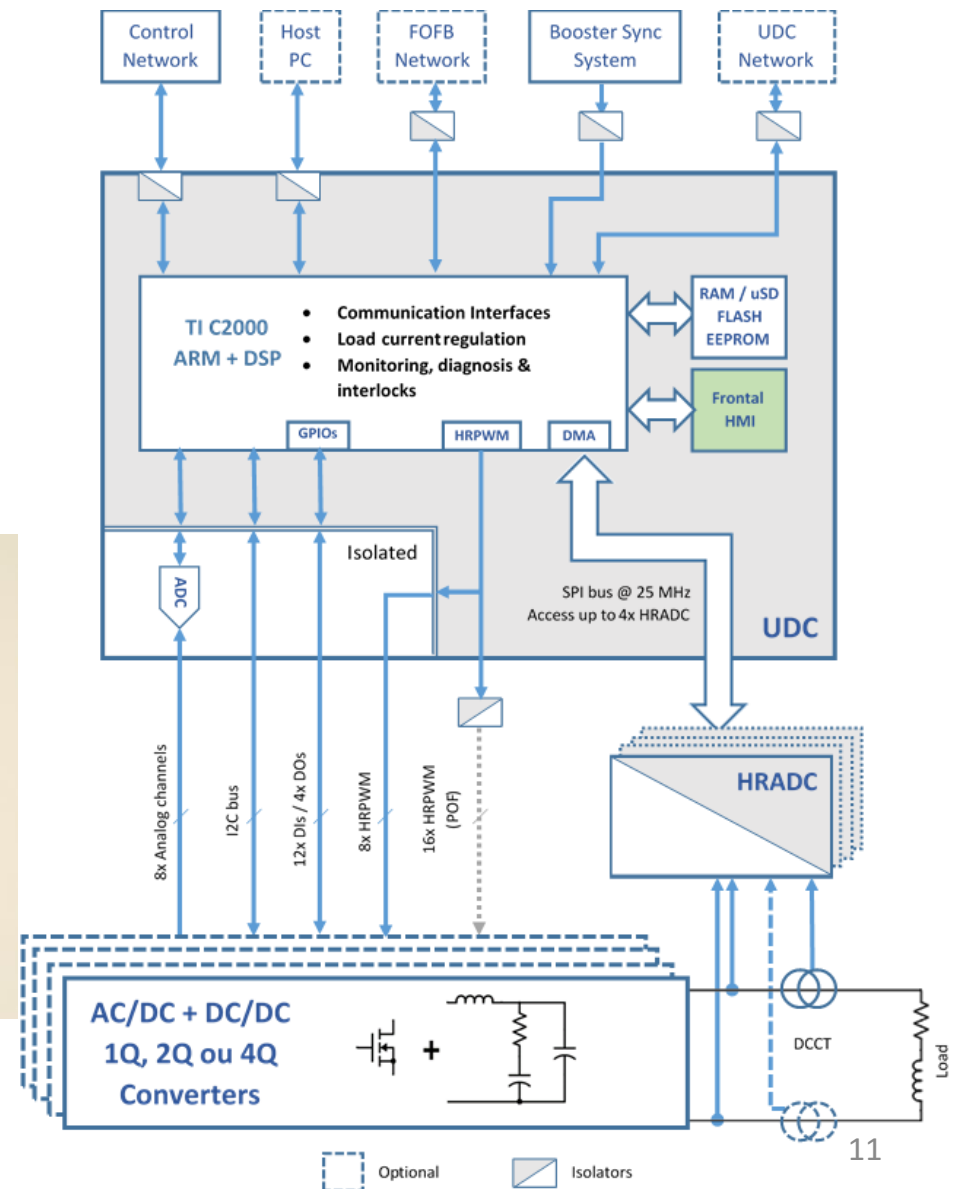
- The same hardware for all PS models
- Completely developed by LNLS, with a initial partnership with the University of Campinas
- Two prototypes already built and tested, and already been used to control the PS prototypes
- Mounting problems with different manufacturers
- Two main boards: *UDC + HRADC*



UDC



HRADC

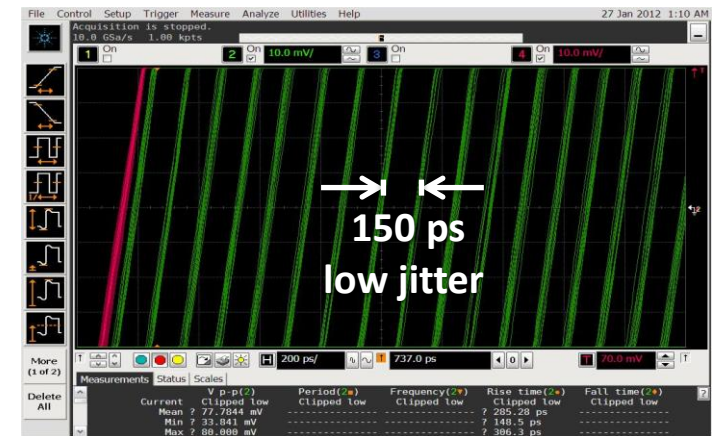




### 2.2 DIGITAL REGULATION SYSTEM (DRS)

#### UDC - UNIVERSAL DIGITAL CONTROLLER

- Based on dual-core microcontroller TI F28M36
- 10 Mbps RS-485 + 10/100 Ethernet interfaces
- 16x HRPWM (150-ps resolution) – 8 isolated channels
- 16x Digital Inputs / 4x Digital Outputs (isolated)
- 8x 12-bit Analog Channels ( $\pm 10$  V isolated)
- 2 multi-purpose synchronization inputs (backplane)
- On-board memories for PS parameters, waveforms, event logger and postmortem buffer



#### HRADC - HIGH RESOLUTION ANALOG-TO-DIGITAL CONTROLLER

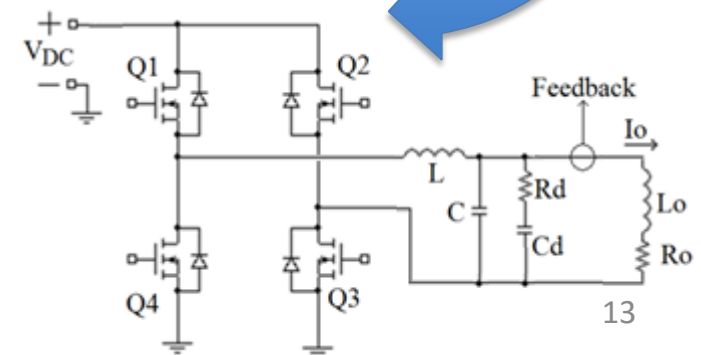
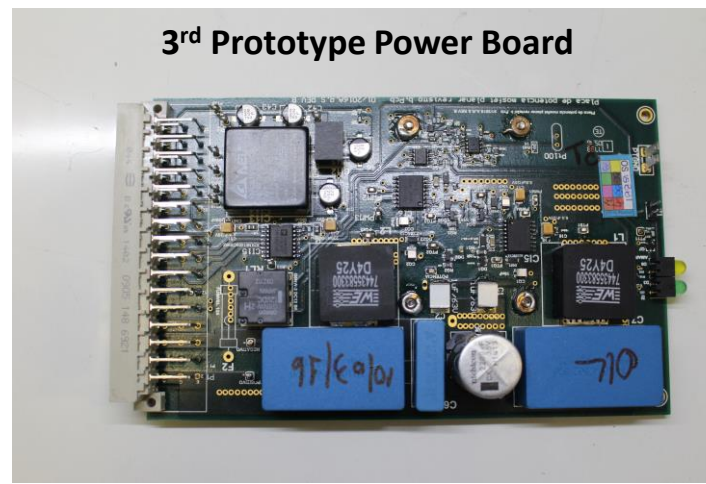
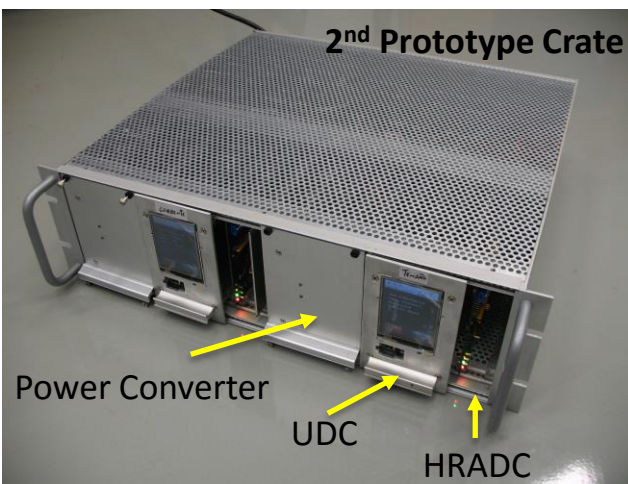
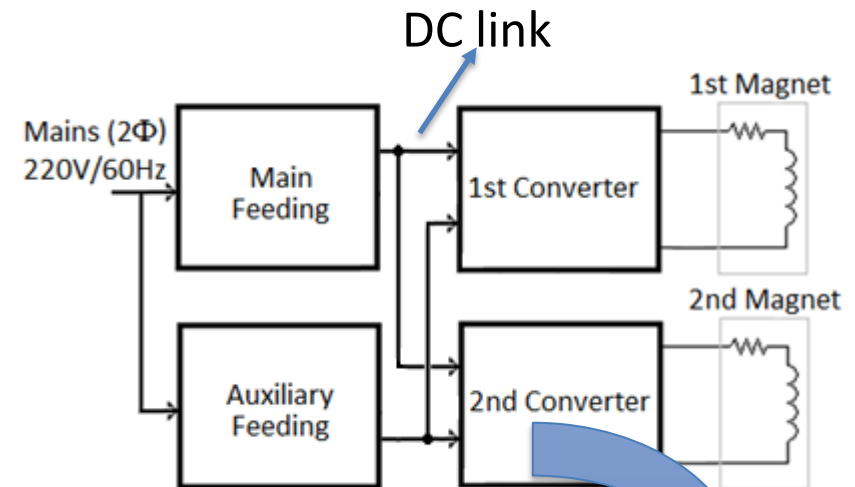
- 18-bit SAR Analog Devices ADC
- Up to 600 kSPS
- Slave-SPI Interface @ 25 MHz
- 1<sup>st</sup>/2<sup>nd</sup> order anti-aliasing filter
- Muxed analog input (for varied DCCT output types)
  - Fully differential voltage input ( $\pm 10$  V)
  - Current input (2.5 ppm/ $^{\circ}$ C bulk metal foil burden)
- 1 ppm/ $^{\circ}$ C voltage reference

#### HRADC v1.1 prototype results

Parameters	$V_{IN}$	$I_{IN}$
24-h stability [ppm]	3.4	4.6
Temp. drift [ppm/ $^{\circ}$ C]	0.83	1.97
10-d gain stability [ppm]	10	22
10-d offset stability [ppm]	5.3	7
TC gain [ppm/ $^{\circ}$ C]	1.44	4.9
TC offset [ppm/ $^{\circ}$ C]	0.8	0.8
Linearity [ppm]	1.5	2.6
Noise RMS [LSB]	0.7	1.8

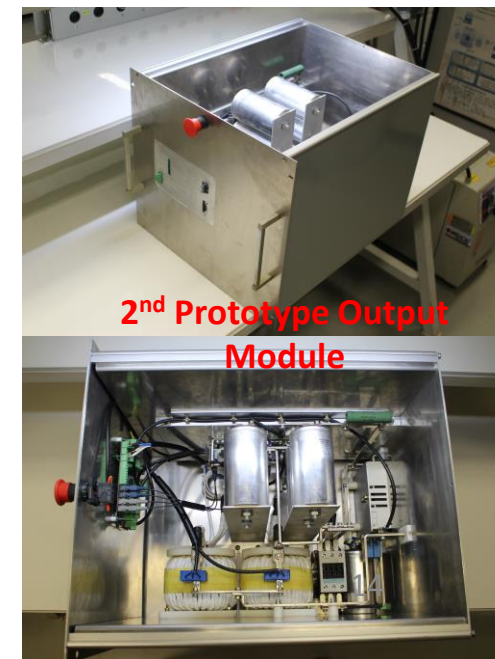
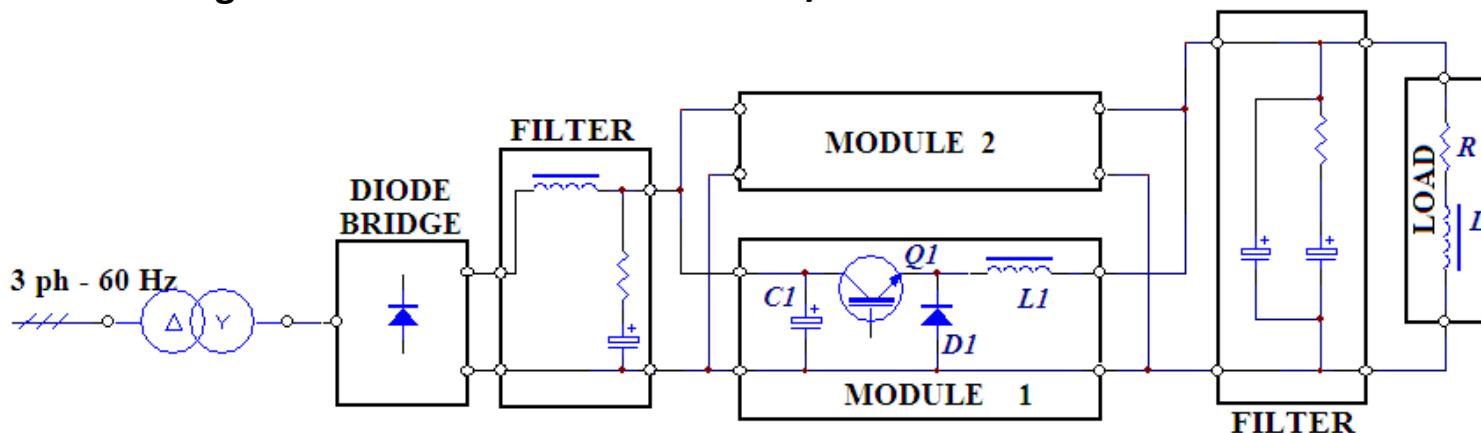
### 2.3 LOW POWER PS (FBP)

- 10A/10V, Bipolar
- Based on Full-bridge as DC/DC converters
- Off-the-shelf solutions for both Auxiliary and Main AC/DC converters
- DC-link can be adjusted according to the maximum output voltage
- Two versions of prototypes built and tested (2 units/crate)
- 10 units of 2<sup>nd</sup> prototype will be installed soon in the present accelerator (UVX)
- 3<sup>rd</sup> prototype: Right now been tested (4 units/crate)
- Manufacturers are been tested to assembly the PS



### 2.4 HIGH POWER PS (FAP)

- Based on 2 Buck converters operating in parallel with interleaved trigger
- Water cooled
- 1<sup>st</sup> Prototype (225A/22.5V): built and tested
- 2<sup>nd</sup> Prototype (200A/200V):
  - DC/DC converter built, finishing the AC/DC converter
  - After tests 3 units will be used to feed the sextupoles of UVX
  - New strategies of control (feedforward, double control loop) will be used to better the instabilities due to input voltage variations
- Storage Ring Dipole PS will use 4 units series-parallel associated of the same modules
- Depending on the available time a lower module (150A/120V) will be designed for those PS that need 150A/120V

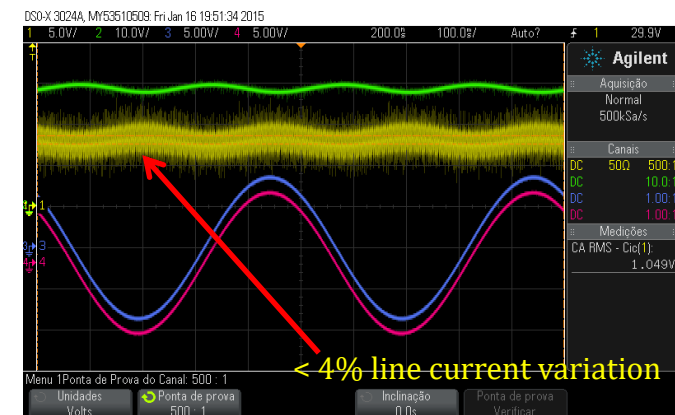




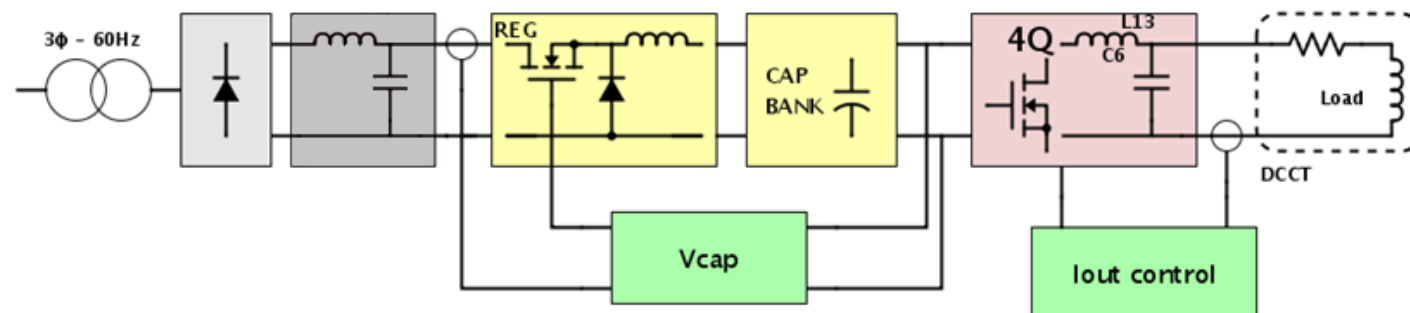
## 2. SIRIUS POWER SUPPLIES

### 2.5 AC POWER SUPPLY (FAC)

- Must follow a 2-Hz waveform (sinusoidal or triangular, not yet defined)
- Two stages:
  - ✓ Input Stage (Buck converter): responsible by avoiding the 2-Hz in the grid and to control the average voltage in the capacitor bank
  - ✓ Output Stage (Full-bridge): responsible by the output current follow the reference with low error, 4-quadrant operation
- First Prototype (130A/10V)
  - ✓ Built, tested and presently being used by Magnet Group to test magnets
- Second Prototype (1.1kA/70V)
  - ✓ Two 550A/70V modules operating in parallel, with interleaving
  - ✓ Been tested right now
- Dipole PS: (1.1kA/900V)
  - ✓ Four 550A/450V modules operating in series-parallel, with interleaving



Ch1: Input Current (5A/div)  
Ch2: Cap Bank Voltage (10V/div)  
Ch3: Output Current (75A/div)  
Ch4: Input Reference (75A/div)



## THE MAIN PERFORMANCE PARAMETERS OF PS

- Few parameters already calculated and specified by physicists
- Some defined by ELP Group
- How to measure some parameters, mainly for greater PS?

### Main PS performance parameters

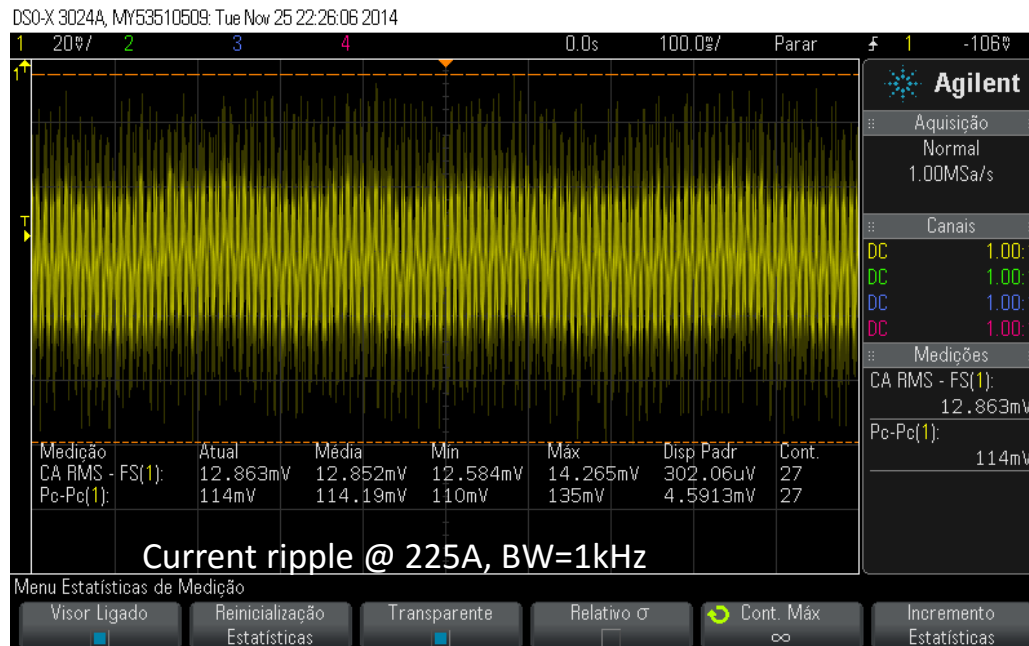
	FAP	FAC	SLOW FBP	FAST FBP
RMS ripple @ BW [ppm @ Hz-kHz]	20 @ 0.1-3	100 @ 0.1-3	20 @ 0.1-3	100 @ 1-100
12h stability [ppm]	20	100	100	100
Accuracy [ppm]	200	500	500	500
Resolution [bits]	18			
Crosstalk [ppm]	20	-	20	20
Bandwidth @ Ipp [Hz @ ppm]	50 @ 1000	500 @ 1000	100 @ 1000	3k @ 1000
Tracking error [ppm]	-	100	-	-
Holding Time [s]	0.05	0.01	0.05	0.05
Minimun Power Factor	0.92			
Minimun Efficiency	0.8	0.7	0.7	0.5

\* All measurements in ppm are in relation to the nominal output current of the PS

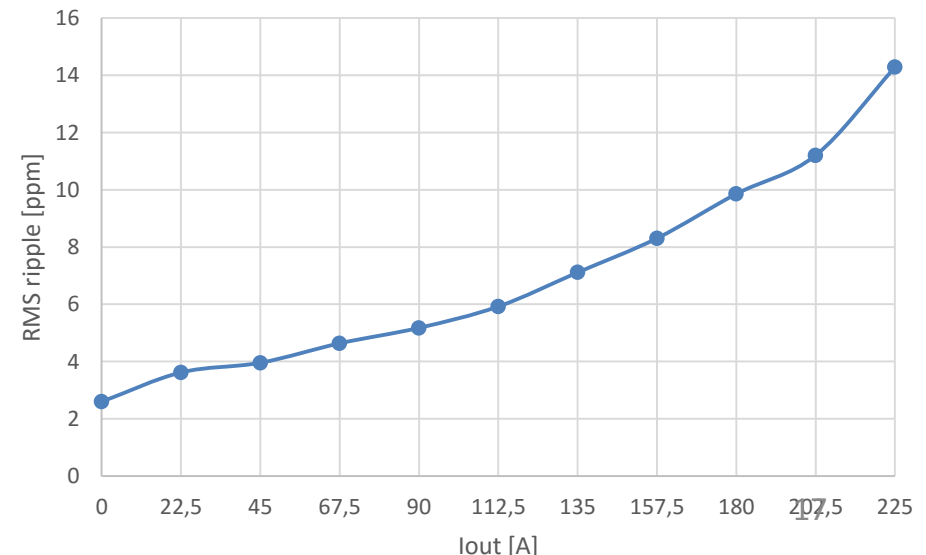
## I. OUTPUT CURRENT RIPPLE (RIP) [ppm @ Hz-Hz]

- Definition: The rms ripple of the output current considering the components from a lower frequency (e.g. 0.1Hz) to a upper one (e.g.: 3kHz)
- Procedure:
  - The output current is adjusted each 10% of its nominal value
  - It is measured using an external DCCT connected to a Differential Amplifier (Tektronix AM502), where the BW is selected
  - The output of the Amplifier is connected to a Digital Scope (Agilent DSO-X 3024A), which shows the waveform and measures its RMS value

### Example of measurements - FAP



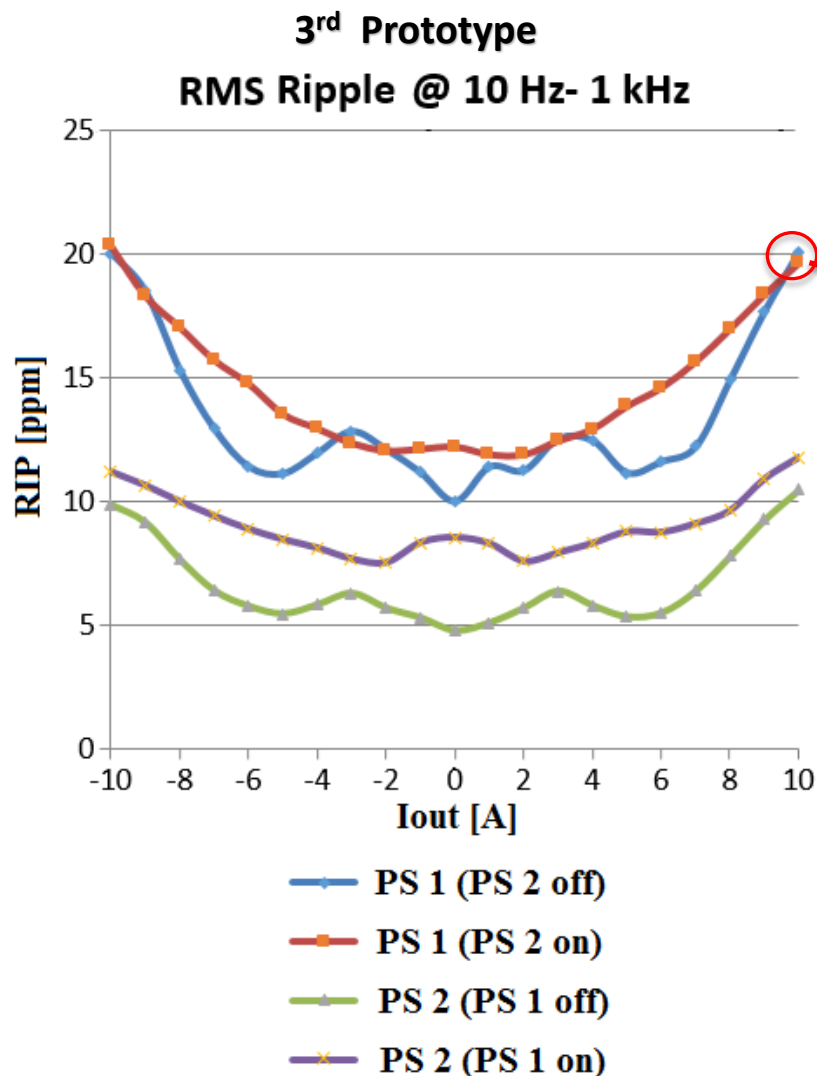
Ripple RMS @ DC - 1kHz



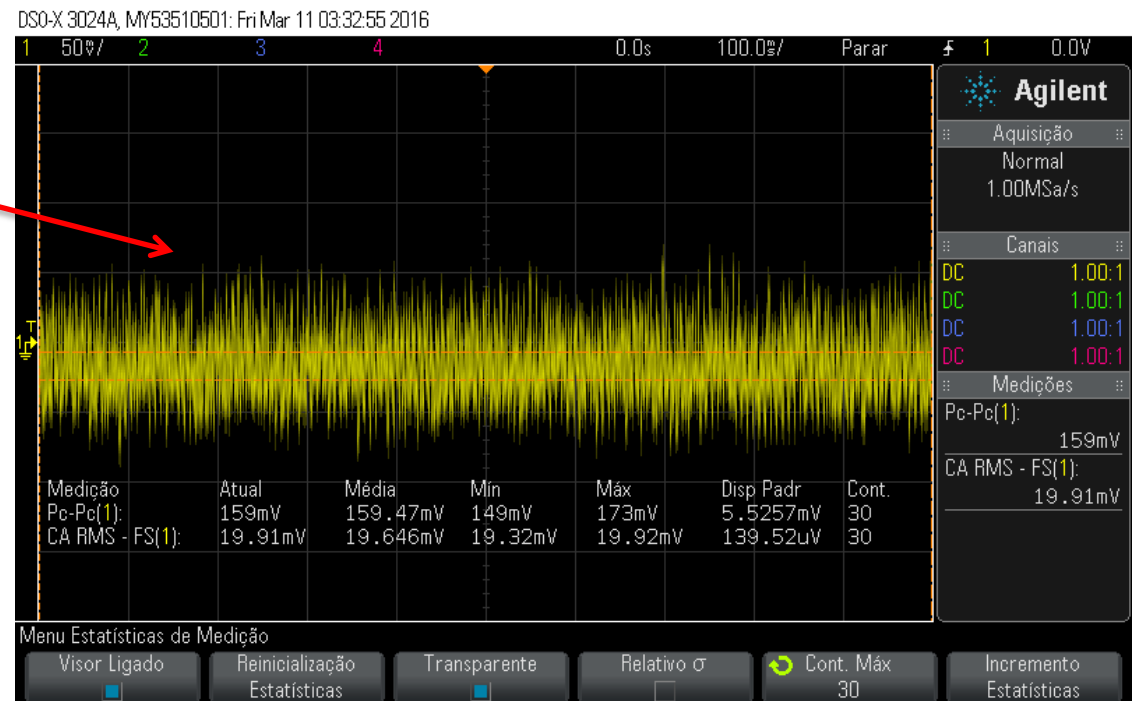


## I. OUTPUT CURRENT RIPPLE (RIP) [ppm @ Hz-Hz]

### Example of measurements - FBP



### 3<sup>rd</sup> Prototype: Ripple PS 1 @ +10A (PS 2 on)

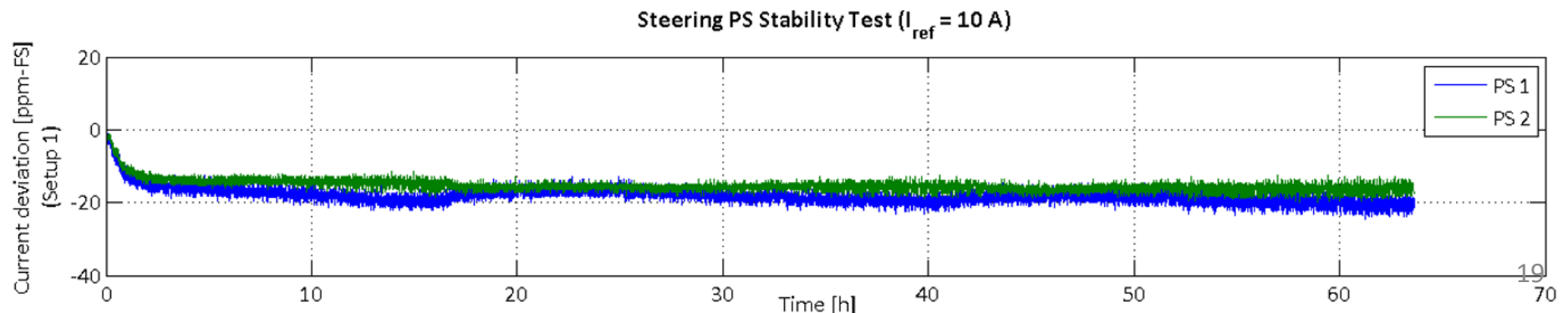


## II. 12-h STABILITY (STB) [ppm]

- Definition: The maximum variation in the output current average (?) , along a 12 hours test with controlled temperature (e.g. +/-0.5°C) and fixed operation point
- Procedure:
  1. The output current is adjusted to 10%, 50% or 100% (1-Q) or 0% and +/-100% (4-Q) of its nominal value
  2. It is measured using an external DCCT connected to a 6 ½ digit acquisition multimeter (Agilent 34970A), where the line cycles of integration is selected 100 NPLC
  3. Usually the test is started just after to turn on the PS, in order the warm-up time can be measured in the same test
  4. The stability is the difference between the maximum and minimum measured value during the last 12 hours of the test

### Example of measurements – 1<sup>st</sup> prototype FBP

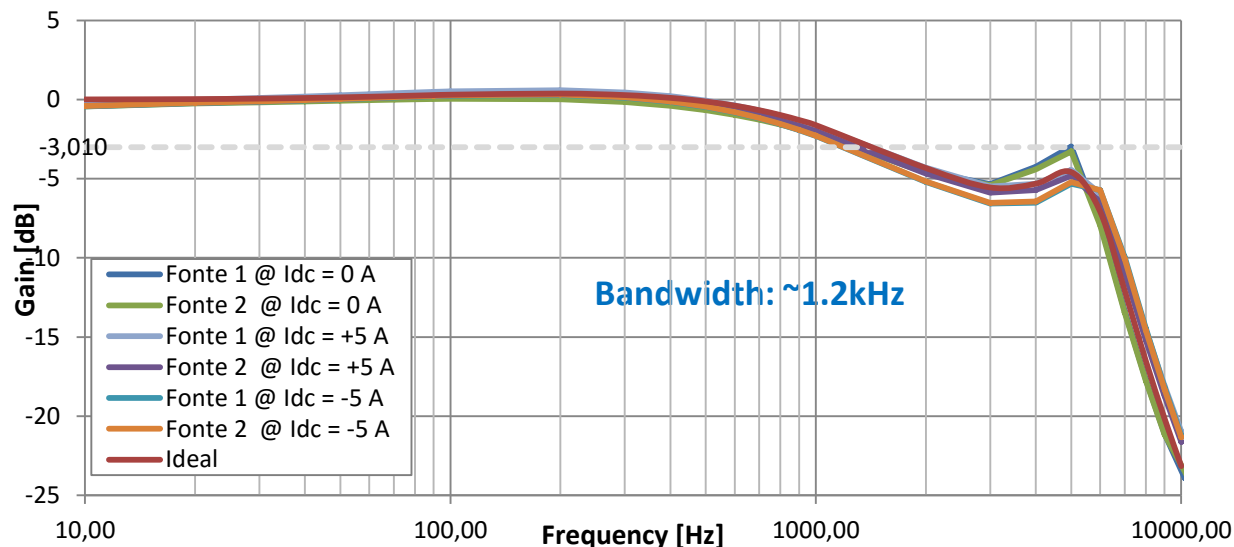
- Stability: <33.5ppm
- Warm-up: <3h



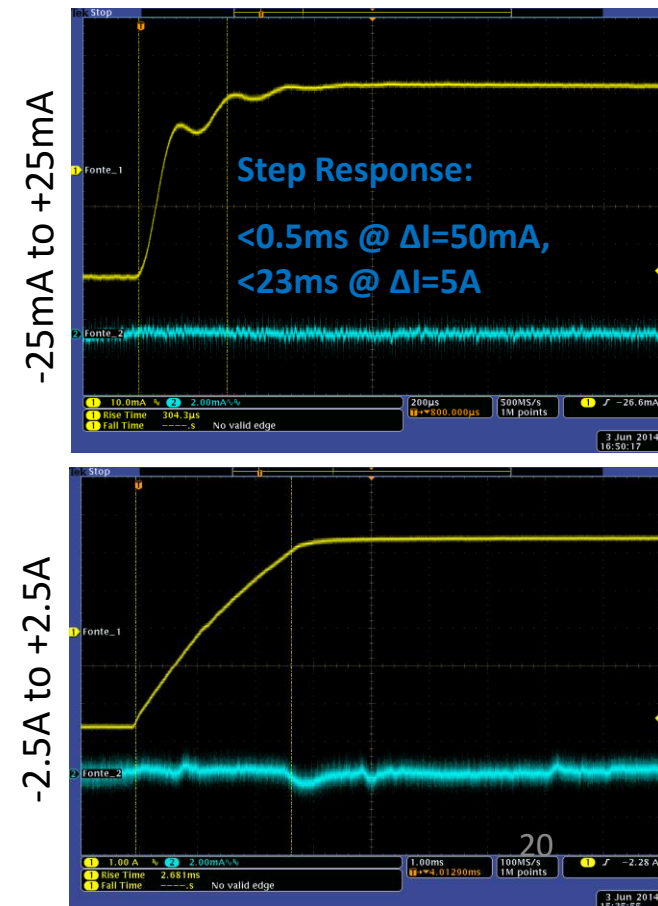
## III. BANDWIDTH (BW) [Hz]

- Definition: The upper limit of the frequency range which the PS is able to follow a sinusoidal reference with peak-to-peak value  $I_{pp}$  with a gain higher than -3dB
- Procedure: a sinusoidal reference is generated by the waveform generator of the UDC and the frequency is adjusted very slowly from 10Hz to 10kHz, and the RMS value of the output current is measured with 6 ½ digit acquisition multimeter
- The phase is not measured (no appropriated equipment)
- Usually a step response test is also performed to check the results (0.5%, 5% and 50% of  $I_{nom}$ )

FBP 1<sup>st</sup> Prototype Frequency Response



FBP 1<sup>st</sup> Prototype Step Response

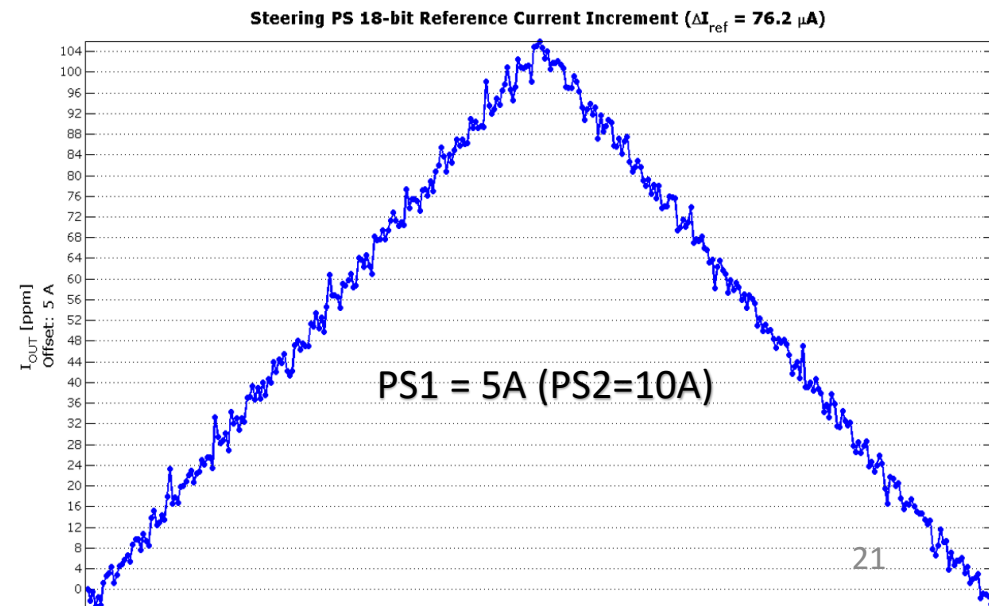
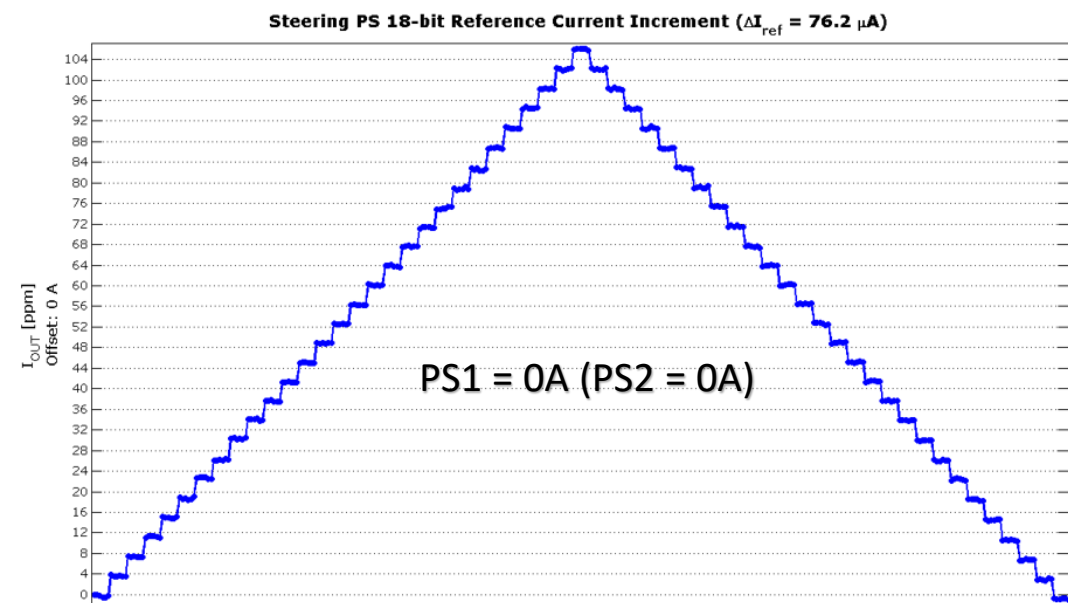




## IV. RESOLUTION (RSL) [bits]

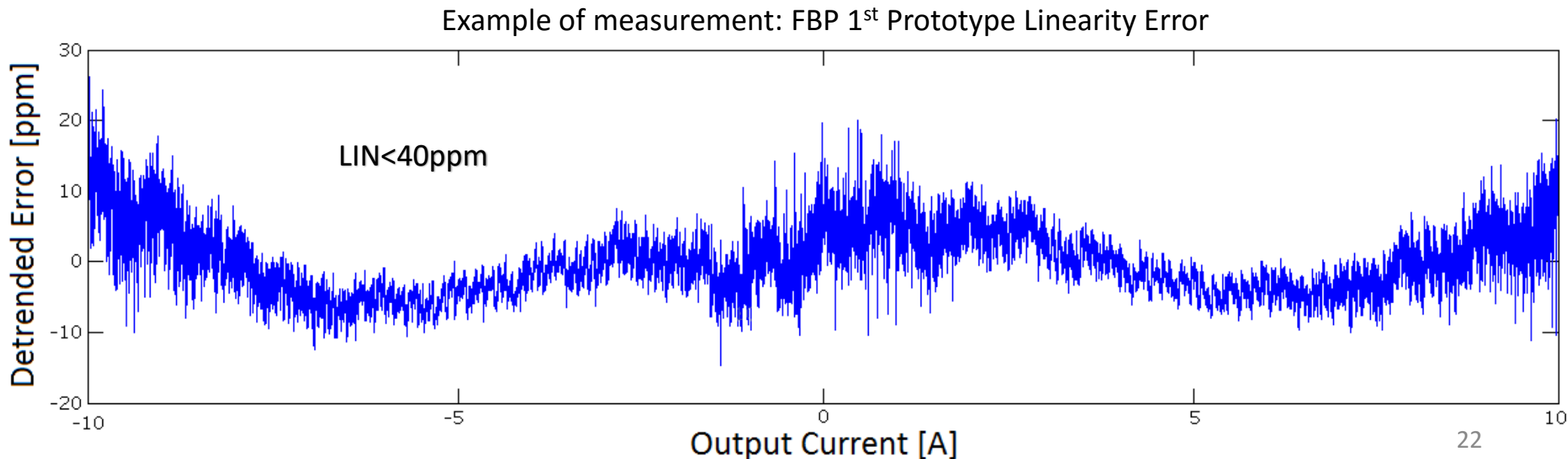
- Definition: The number of bits that can be used to form the digital reference value and still obtain a monotonic answer
- Procedure:
  1. The UDC increments the reference in one LSB each 5 seconds close to a chosen set point (0 and +/-50% of the nominal current)
  2. A 6 ½ digit acquisition multimeter measures the output current each one second with a integration time of 20 NPLC

Example of measurement: FBP 1<sup>st</sup> Prototype



## V. LINEARITY (LIN) [ppm]

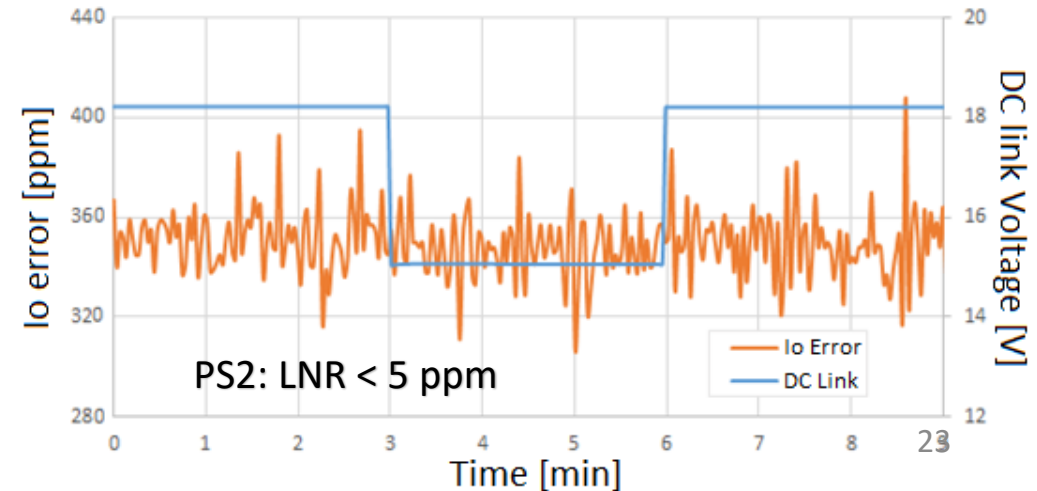
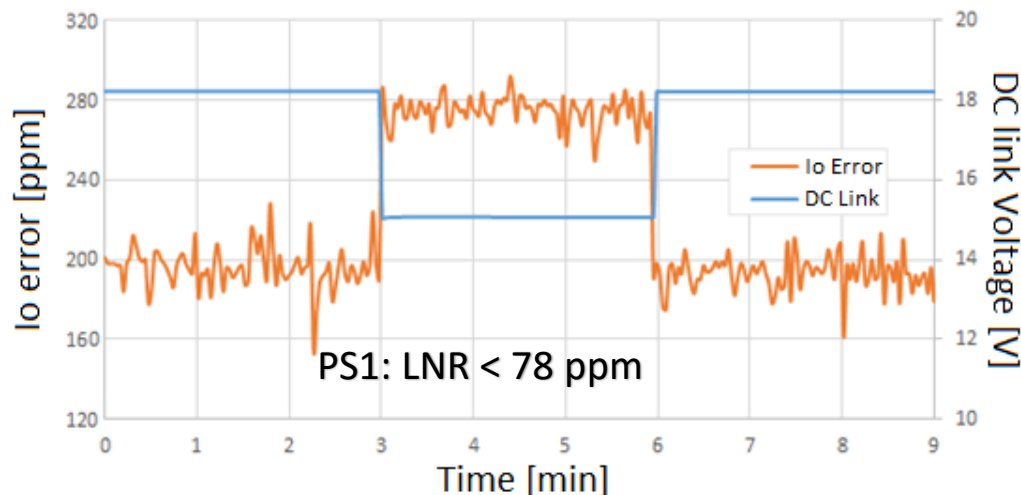
- Definition: the variation in the error between reference and output current, in ppm, discounting the gain and offset error
- Procedure:
  1. The output current is adjusted from the minimum to the maximum value in fixed steps (e.g. 1000ppm), staying in this value for 5 seconds
  2. The output current is measured for each reference value and calculated the error
  3. The plot of the error is linearized and the difference between this error and the “real” one is calculated and plotted.
  4. The difference between the minimum and maximum value of this graphic is the linearity error.



## VI. LINE REGULATION (LNR) [ppm]

- Definition: the variation in the output current, in ppm, due to a step in the line voltage
- Procedure:
  1. The PS is connected to grid with a series resistance which value is enough to cause a 20% voltage drop when the nominal current is adjusted in the output
  2. With the resistance short-circuited, the output current is adjusted to the nominal value (both negative and positive, if 4-Q)
  3. The output current is measured with a 6 ½ digit acquisition multimeter
  4. The short-circuit across the resistance is taken away and after 30 seconds placed again
  5. The difference in the average value of the output current in both situations is the line regulation
  6. It is also observed with a scope the variation in the output current during the transient

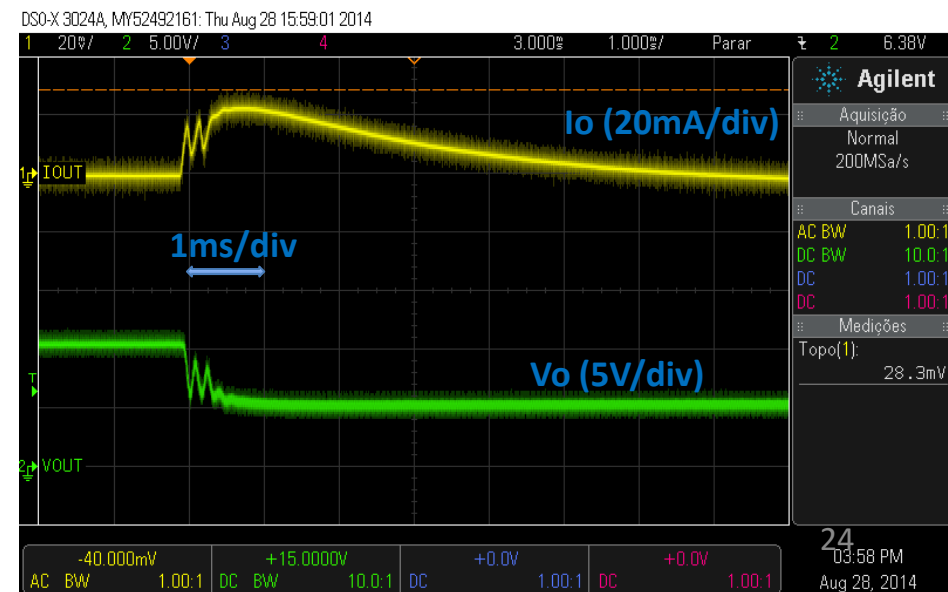
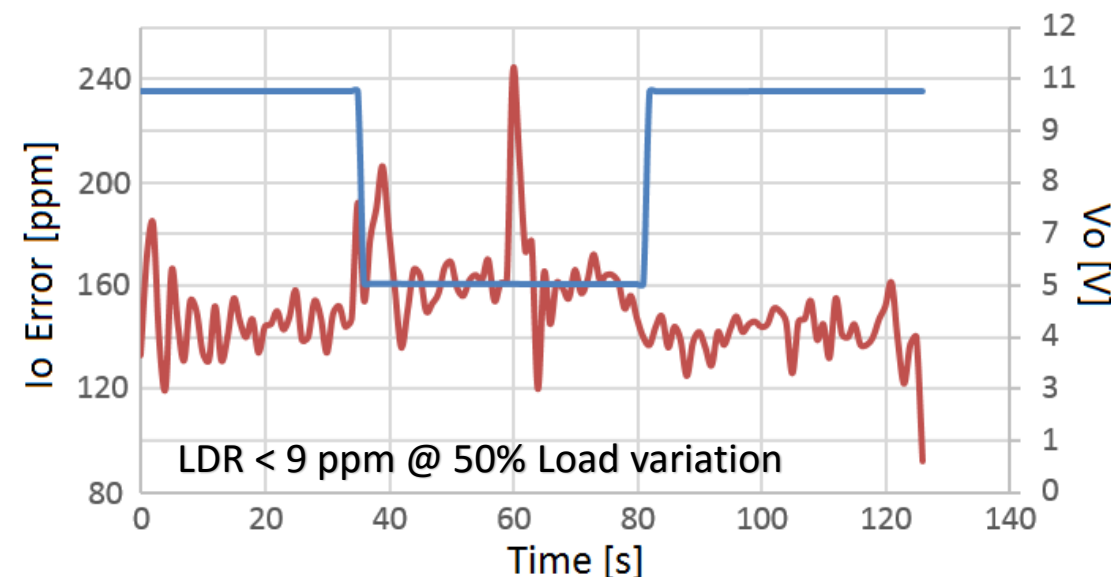
#### Example of measurement: FBP 1<sup>st</sup> Prototype with 10A



## VII. LOAD REGULATION (LDR) [ppm]

- Definition: the variation in the output current, in ppm, due to a step in the load resistance
- Procedure:
  1. The output current is adjusted to the nominal value (both negative and positive, if 4-Q)
  2. The output current is measured with a 6 ½ digit acquisition multimeter
  3. Part of the load resistance is short-circuited in order to reduce the total load resistance (e.g. to 50%) and after approximately 30 seconds returned to the initial value
  4. The difference in the average value of the output current in both situations is the load regulation
  5. It is also observed with a scope the variation in the output current during the transient

### Example of measurement: FBP 1<sup>st</sup> Prototype with 10A

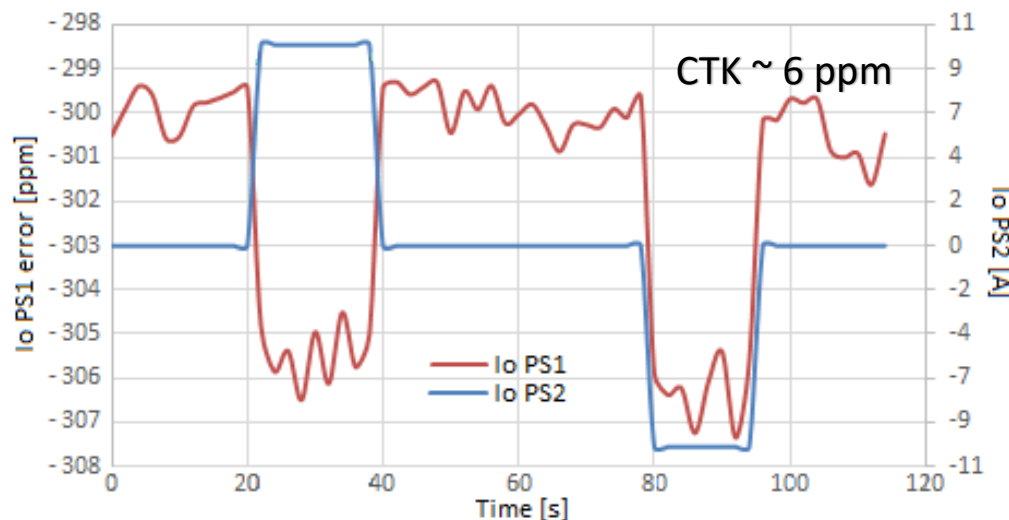




## VIII. CROSS-TALK (CTK) [ppm]

- Definion: The maximum variation in the output current of one PS when another one that shared the same crate or some electrical circuit goes from zero to its maximum value
- Procedure:
  1. Turn on the PS under test and adjust the output value to 0A (1-Q) or 50% of the nominal value (4-Q)
  2. Turn on the other PS and adjust 0A
  3. Measure the output current with a 6 ½ digit acquisition multimeter and wait until it stabilize
  4. Change the output current of the other PS to the nominal value, wait a minute and return it to zero
  5. If this PS is 4-Q, wait some minutes and repeat it for the negative nominal value

**Example of measurement: FBP 1<sup>st</sup> Prototype**



#### IX. HOLDING TIME (HT) [ms]

- Definition: The time that the PS can keep the output current (adjusted in its nominal value) within its specifications, when the input voltage is turned-off
- Procedure:
  1. Adjust the output current to its nominal value
  2. Measure this current with a scope and a Differential Amplifier with the bandwidth adjusted to 0.1Hz – 100kHz
  3. After the warm-up time, disconnect the PS of the grid
  4. The holding time is the time that it takes to the output current to fall a value higher than that specified to 12-h stability (e.g. 20ppm)

#### X. POWER FACTOR (PF)

- Definition: The minimum power factor that the PS must present at the nominal condition
- Procedure:
  1. The output current is adjusted to the nominal value (both negative and positive, if 4-Q)
  2. The input voltage and input current are measured with a scope
  3. Using the math function, the Power waveform is obtained by the multiplying of voltage by current, the average of Power wave form is the Active Power, the Apparent Power is obtained multiplying the RMS voltage by RMS current.
  4. The ratio between Active Power divided by Apparent Power is the Power Factor
  5. If a FAP or FAC PS is under test, then a power analyzer is used, it giving us the value directly

#### XI. EFFICIENCY (EF)

- Definition: The minimum efficiency that the PS must present at the nominal condition
- Procedure:
  1. The output current is adjusted to the nominal value (both negative and positive, if 4-Q)
  2. The input and output current and voltage are measured with a scope
  3. Using the Active Power value obtained in the previous measurement as a input power, the output power is obtained using a multimeter and a current transducer(DCCT)
  4. The ratio between output power divided by the input power is the Efficiency

### XII. TRACKING ERROR (TRK) [ppm]

- Definition: The maximum difference between the output current and the reference while the PS is cycling
- Procedure:
  1. The output current follow a wave form in the input
  2. The input setpoint and the output current are measured with a scope
  3. The maximum difference between both signals is the Tracking Error

### XIII. ACCURACY (ACR) [ppm]

- Definition: The maximum difference between the output current and the waited value, in any situation
- Procedure:
  1. The output current is adjusted to a desired value
  2. The output current is measured with a 6 ½ digit acquisition multimeter and a standard DCCT
  3. The difference between the average value of the output current and the setpoint value is the Accuracy



## 4. CONCLUSIONS

- The development of the PS for Sirius has been satisfactory, but the time is short!
- All the prototypes must be tested and approved until the end of this year in order that the units can be produced along 2017
- The ELP group is trying to create a standard for the definition and measurement of the performance parameters, and every suggestion is very welcomed!
- Still learning with the tests
- Efforts are being made to make measurements more automatically

**QUESTIONS?**

**THANK YOU FOR YOUR  
ATTENTION!**