ASML introduction ALBA

Olivier Balmes

June 11th, 2026

Public

Facts and figures (2025)

€32.7bn

Total net sales

535

Total systems shipped

48	279	208
EUV	DUV	Metrology & Inspection

44,210

Employees (FTE)

>60

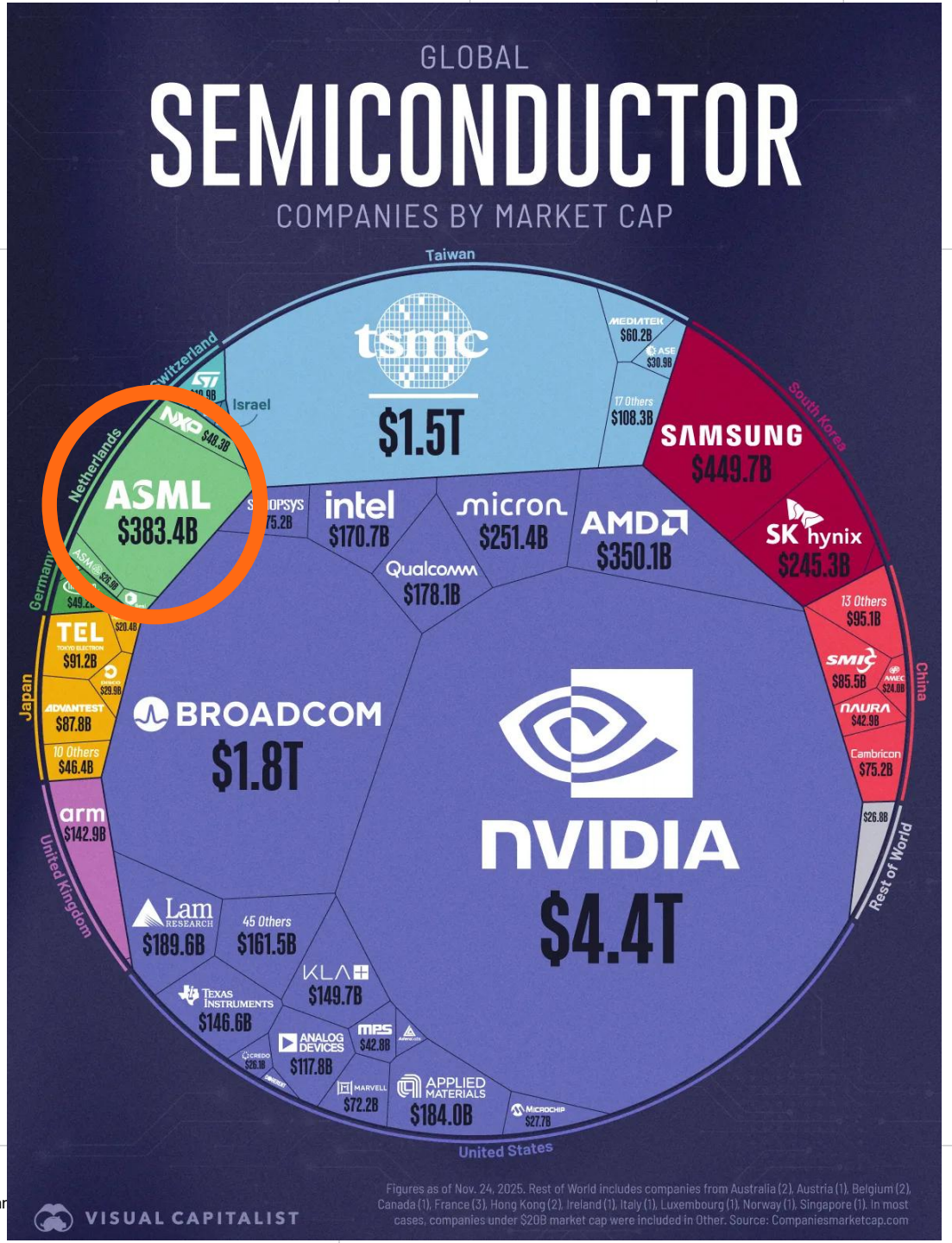
Locations across 3 continents

€4.7bn

Annual R&D investment

8

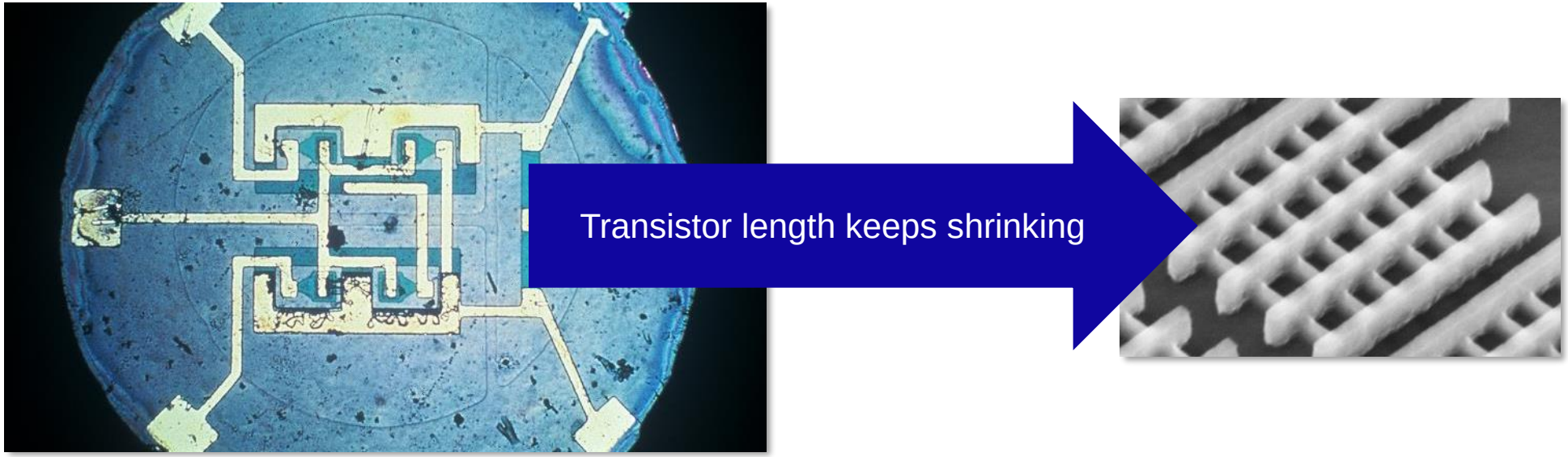
Factories



Based on ASML's 2025 Ann

Public

Key to Moore’s Law: Making smaller transistors



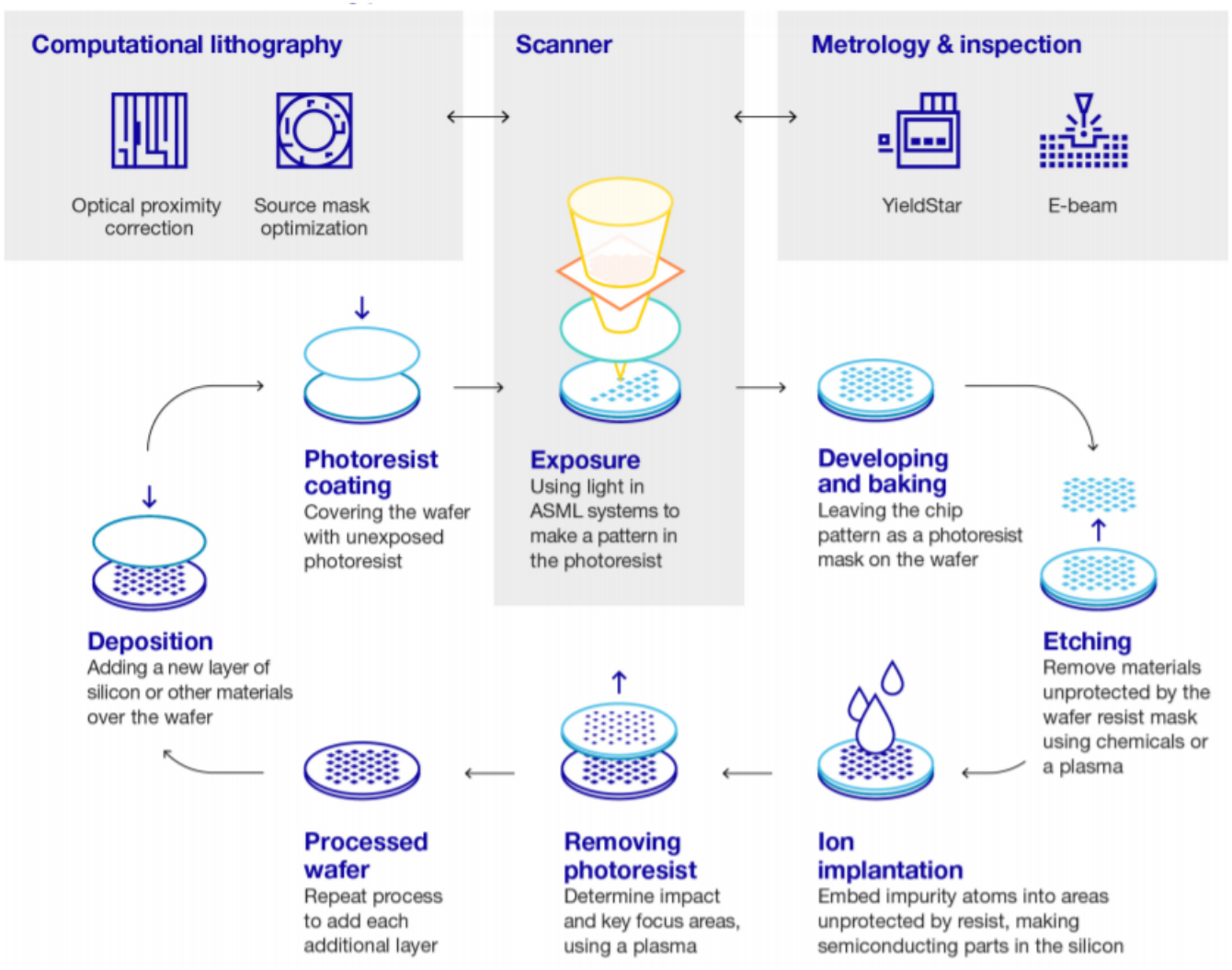
The first integrated circuit on silicon, on a wafer the size of a fingernail

(Fairchild Semiconductor, 1959)

Today: Billions of transistors on the same area

Public

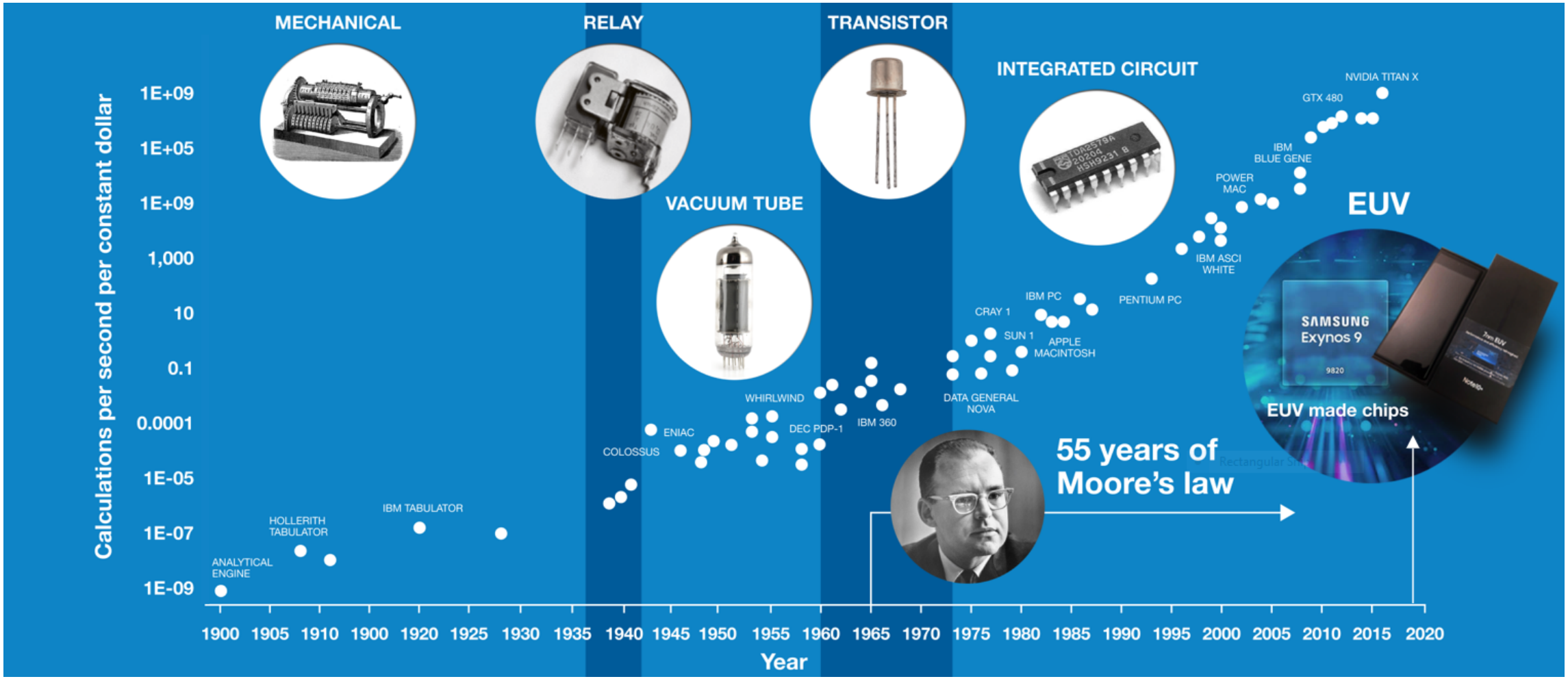
The semiconductor manufacturing loop



Public

The world has been improving computer power for 120 years

18 orders of magnitude increase of calculation speed per dollar, and continuing



Source: Ray Kurzweil, Steve Jurvetson

Public

Shrinking transistors enables more functionality at a lower cost

IBM 5150		Apple iPhone 17 Pro Max
1984	year manufactured	2025
$4700–$9500*	price	$1199–$1999
16-bit Intel 8088 4.77 MHz	processor	Apple A19 Pro chip (3 nm EUV)
29,000	transistor count	~25 billion
16–256 kB	working memory	12 GB
5″ floppy disk, 160 kB	internal storage	up to 2 TB
640 x 200 pixels	display	2868 x 1320 pixels
12.7 kilogram	weight	233 grams

*Adjusted for inflation. At the time, the systems sold for $1500–$3000.

Public

In the world of EUV, everything is bigger

An NXE EUV lithography system…

Has more than 100,000 individual parts, 3,000 cables, 40,000 bolts and 2 km of hosing

Took 20 years of sustained R&D to develop

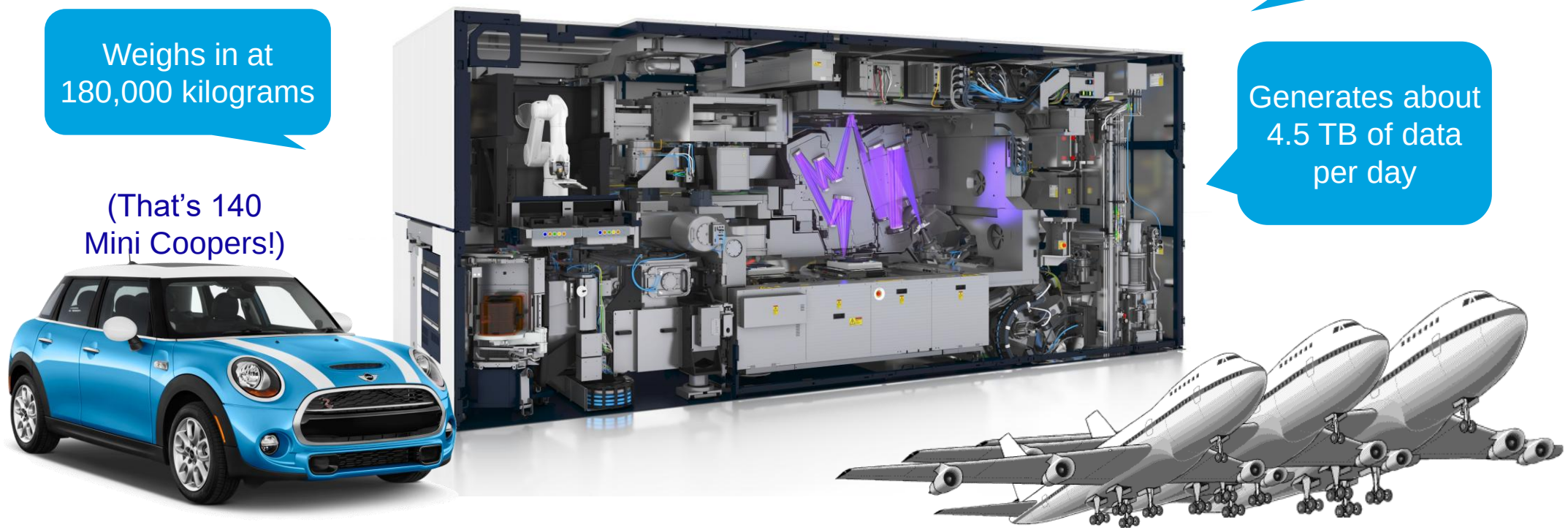
Takes 40 containers, 20 trucks and 3 fully loaded 747s to transport

Has about 1,500 sensors to capture imaging data

Weighs in at 180,000 kilograms

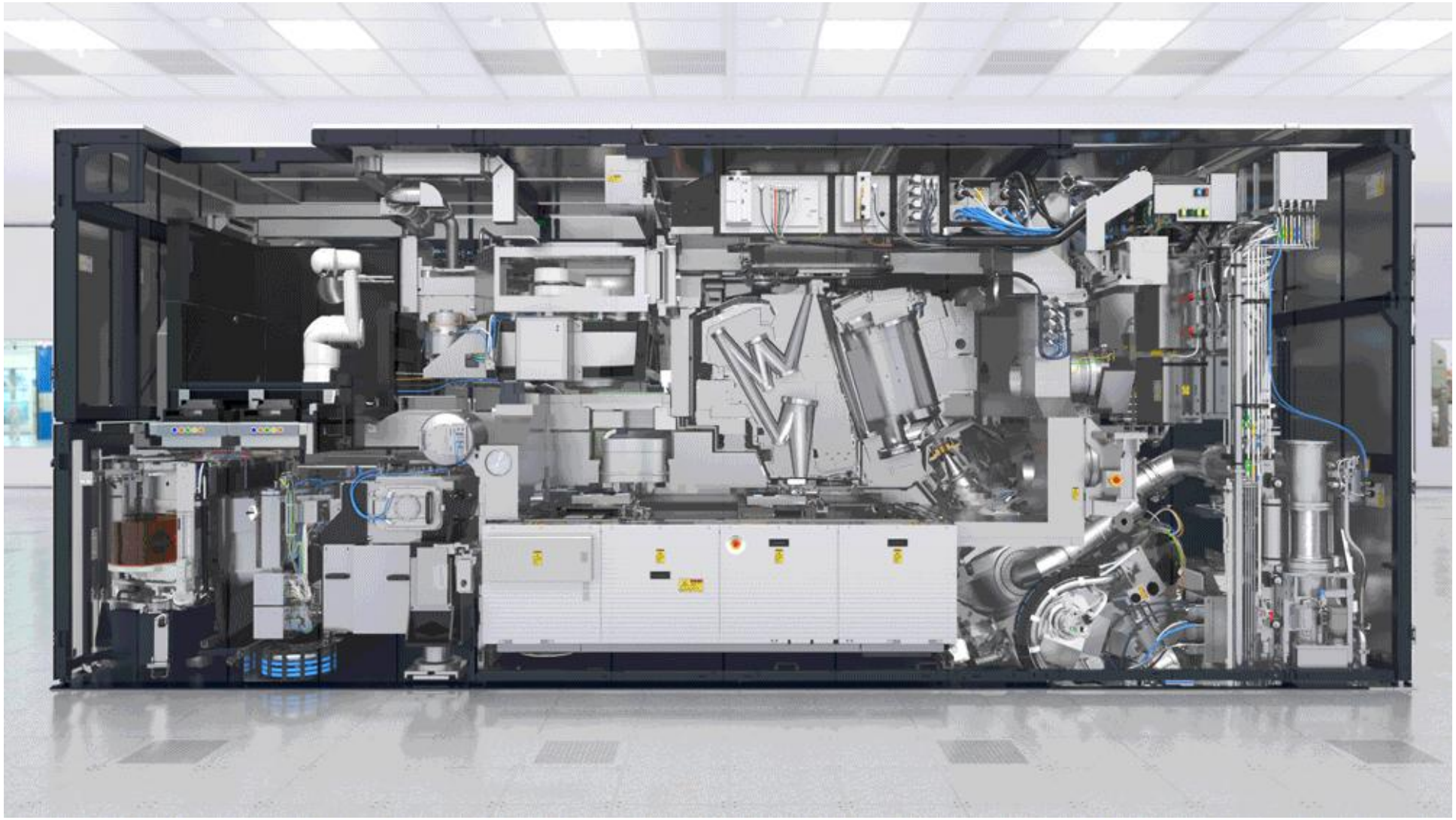
(That's 140 Mini Coopers!)

Generates about 4.5 TB of data per day



Public

How a lithography system works



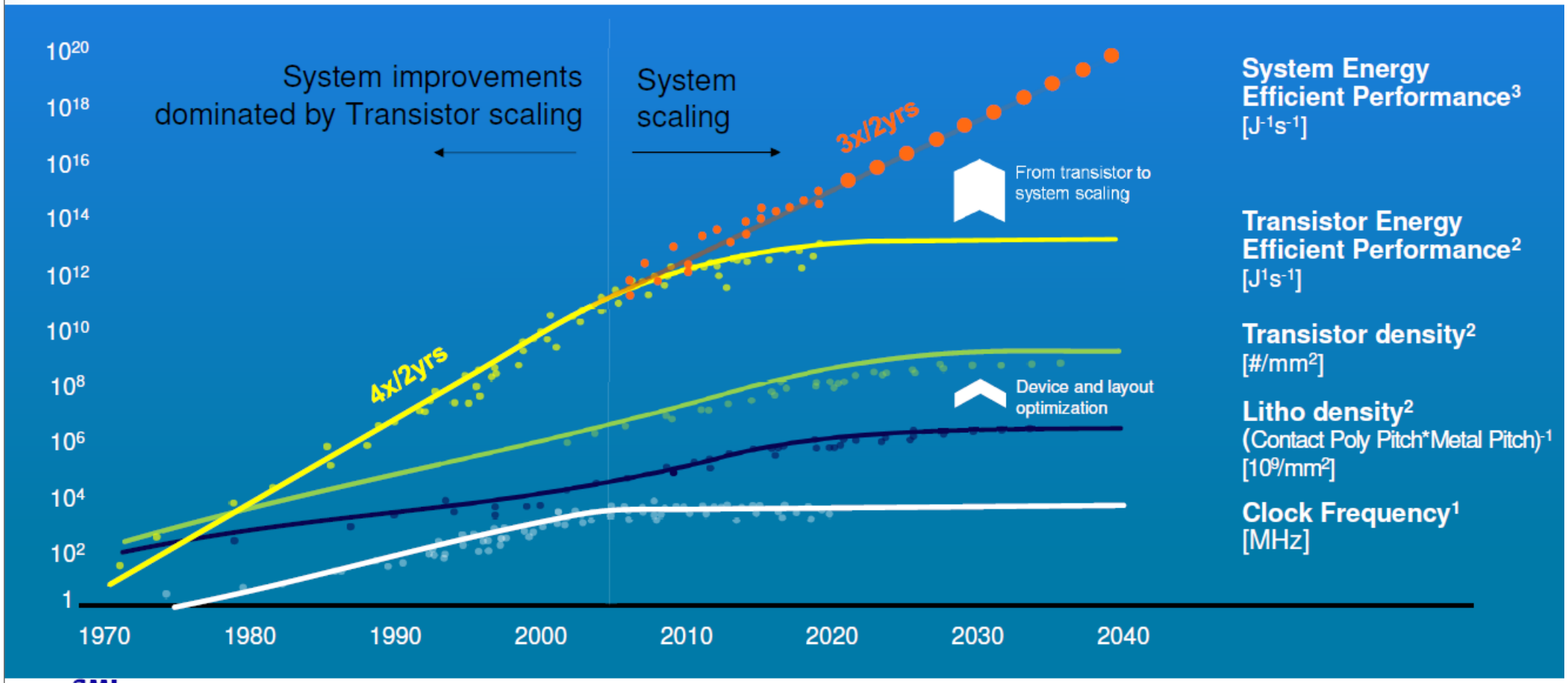
Public

Moore's law evolution: the next 20 years

System scaling to satisfy the need for performance and energy consumption

ASML

Slide 3
TC 2021



Sources: [1]Karl Rupp, [2] ASML data and projection using Rup, [3]Mark Liu TSMC normalized to transistor EEP in 2005

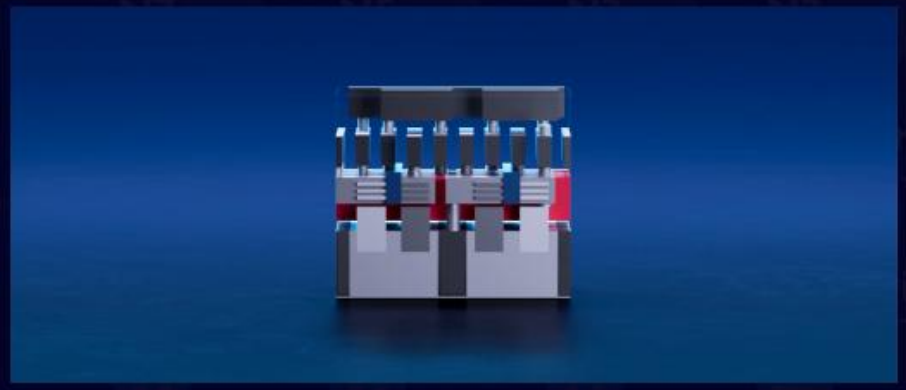
Public

Public

15 years of Logic device innovation and scaling ahead

Device roadmap is translated to litho requirements

Dimensional scaling continues, from Nanosheet to CFET

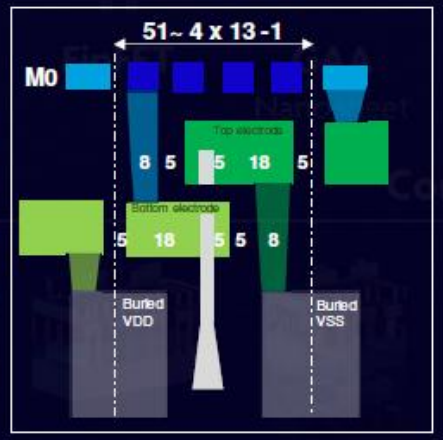


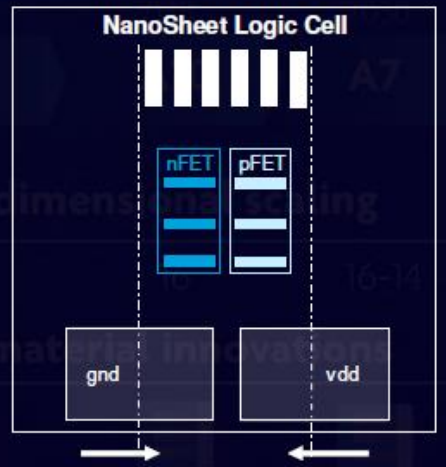
A5" node, HVM 2032

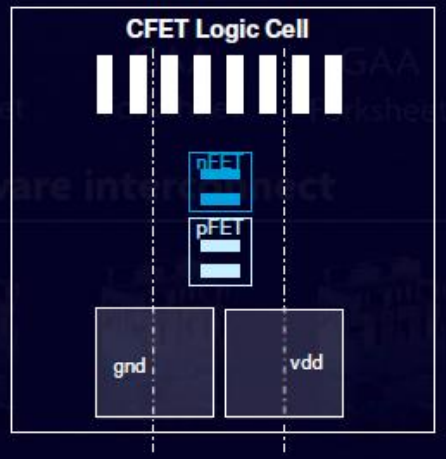
Cell Height ~50nm minimum

Connecting needs 3-4 tracks

Leads to 13nm pitch







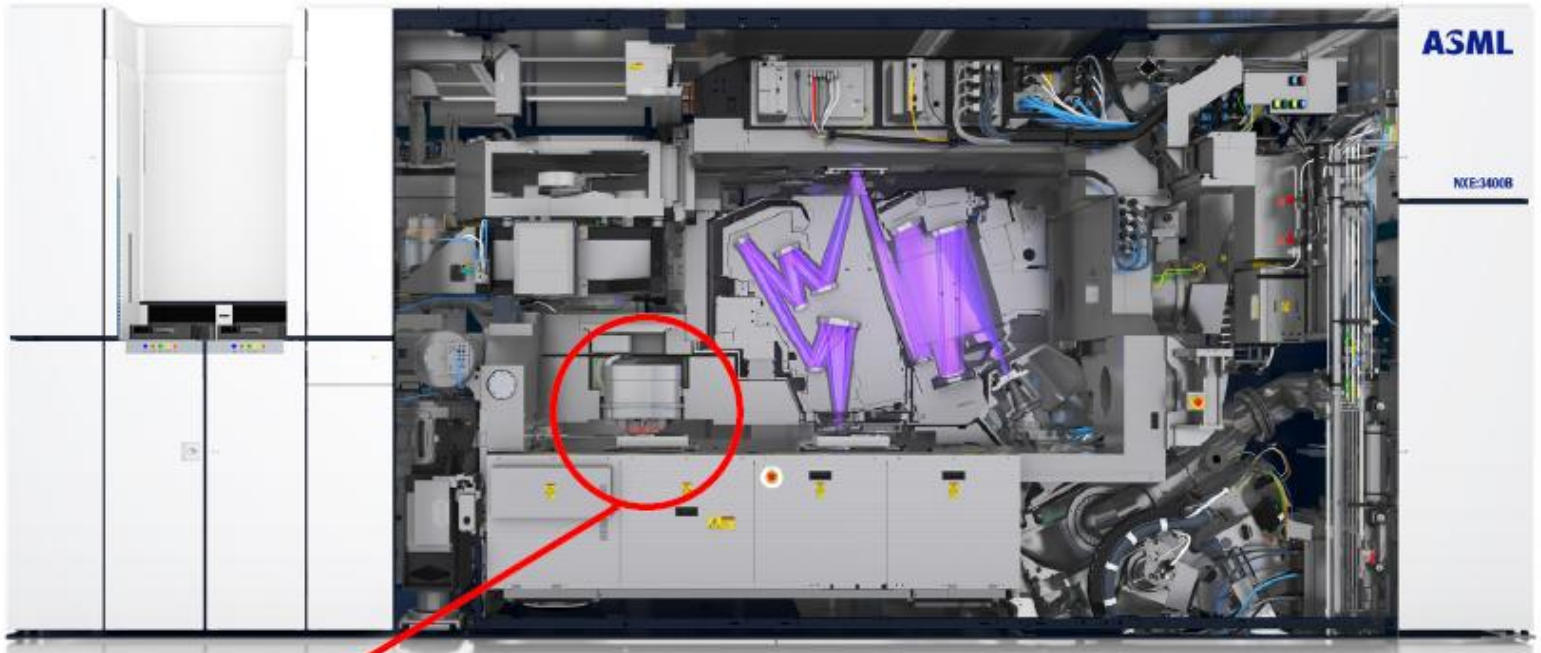
Source: Luc van den Hove, IMEC. "The endless progression of Moore's Law" ISS, April 2022

Public

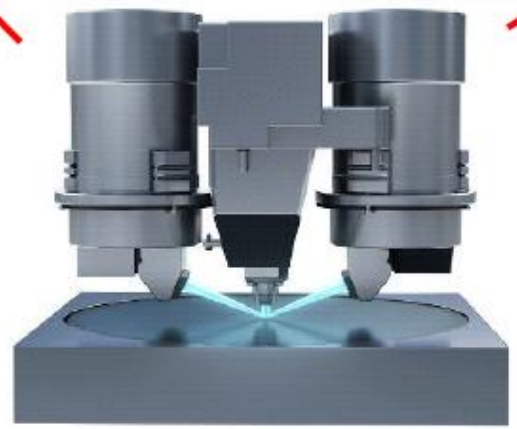
Public

Optical Metrology in the Lithography Scanner

DUV – NXT systems



EUV – NXE systems



Measurement Systems for x-y-z Measurements
(Alignment & Level Sensor)

A lithography tool has 2 critical wafer-metrology sensors:

These sensors are used *before* the wafer is exposed

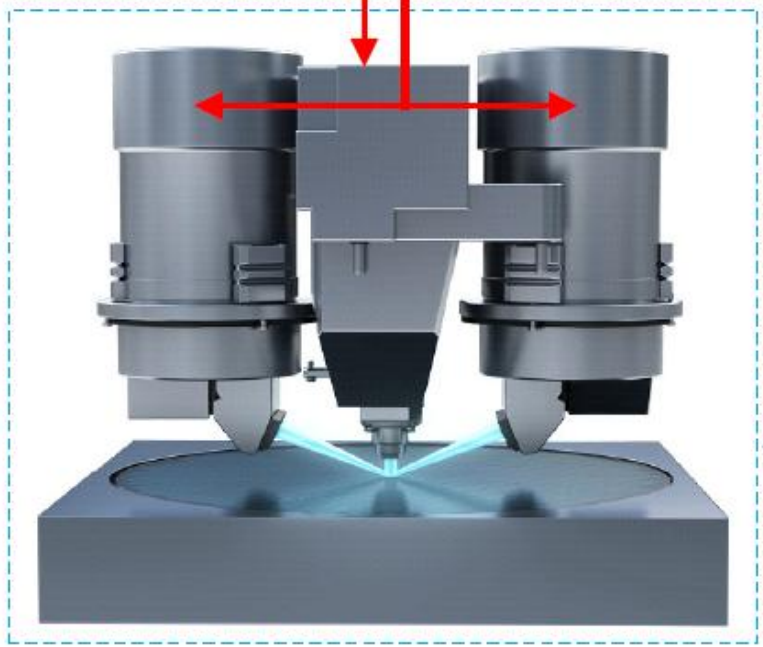
Alignment Sensor:
- Measures wafer *location*
- Critical for OV* performance

OV = overlay

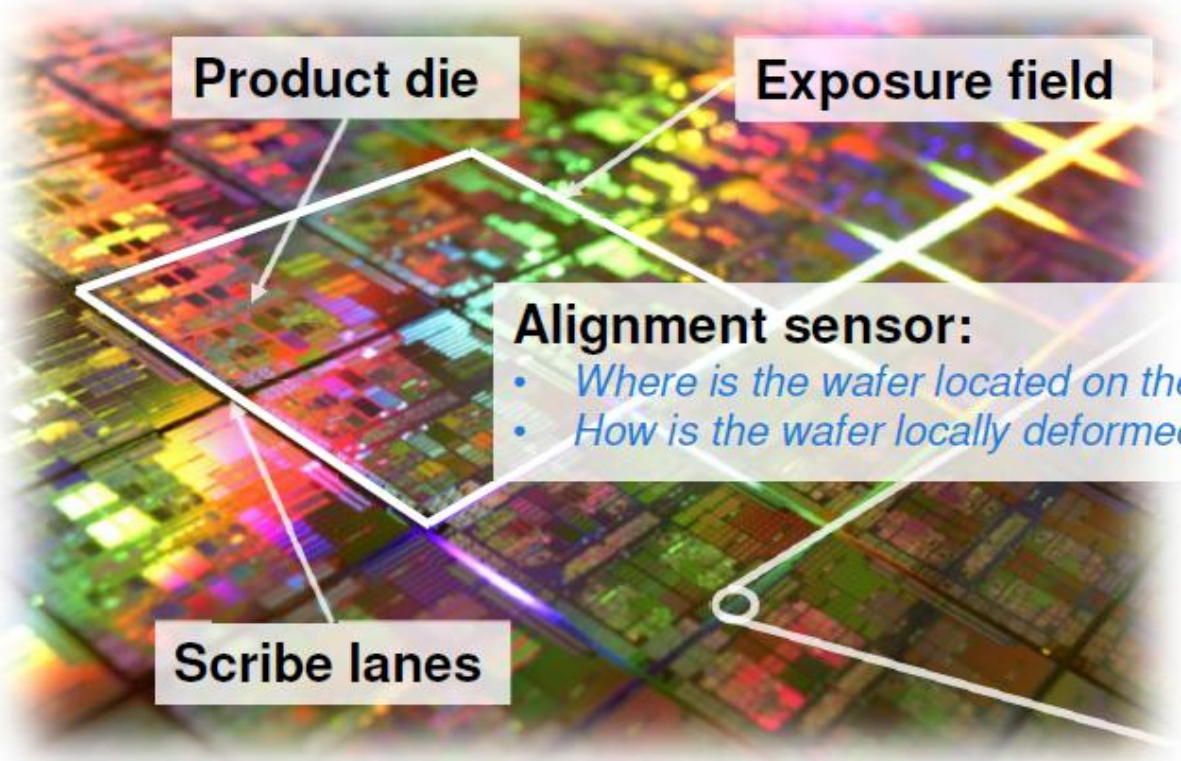
Level Sensor:
- Measures wafer *height*
- Critical for CDU* performance

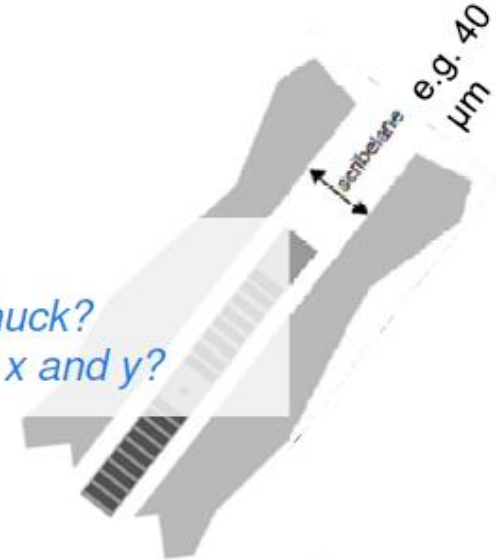
CDU = critical dimension uniformity

Boundary conditions:
- Phase-grating alignment
- Large dynamic range ~ 10^4
- Sub-nm accuracy
- Multiple wavelengths
- Flexibility in grating pitch
- Small spot : < 40 micron
- Working distance < 10mm



Alignment Sensor Challenges

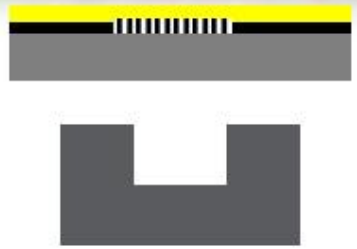




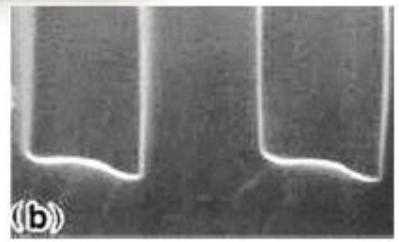
Example of an alignment mark in a scribe lane

Goal:

- Alignment marks as small as possible
- With a pitch as small as possible (preferably similar to product features)
- Read out of 100+ marks per wafer (in ~5 seconds)



This is how we often draw an etched grating



In reality, grating profiles can be asymmetric as shown in this extreme example

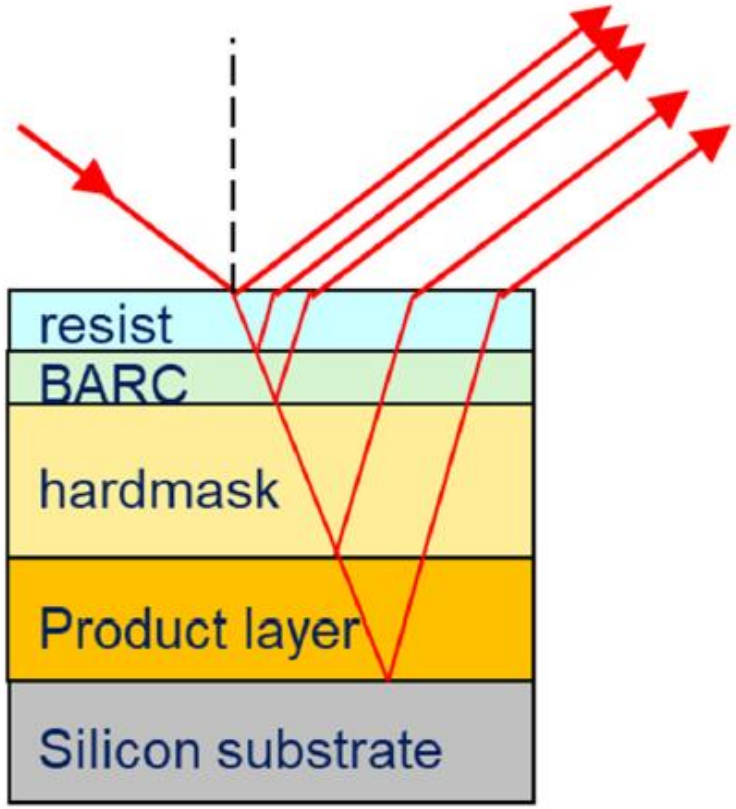
Etched grating profiles can also have asymmetric sidewalls due to "ion beam tilt"

Level Sensor Challenges

Level Sensor works with Triangulation principle

Goal:

- Make height map of full 300 mm wafer at a spatial resolution of ~0.5*1 mm (1e5 data points), to be able to print all features in focus
- At ~nm accuracy
- In ~1 second
- Be robust for process dependency
  - Hardmasks become thinner with new process nodes
  - Focus budgets become tighter, needing more accurate Level Sensor measurements

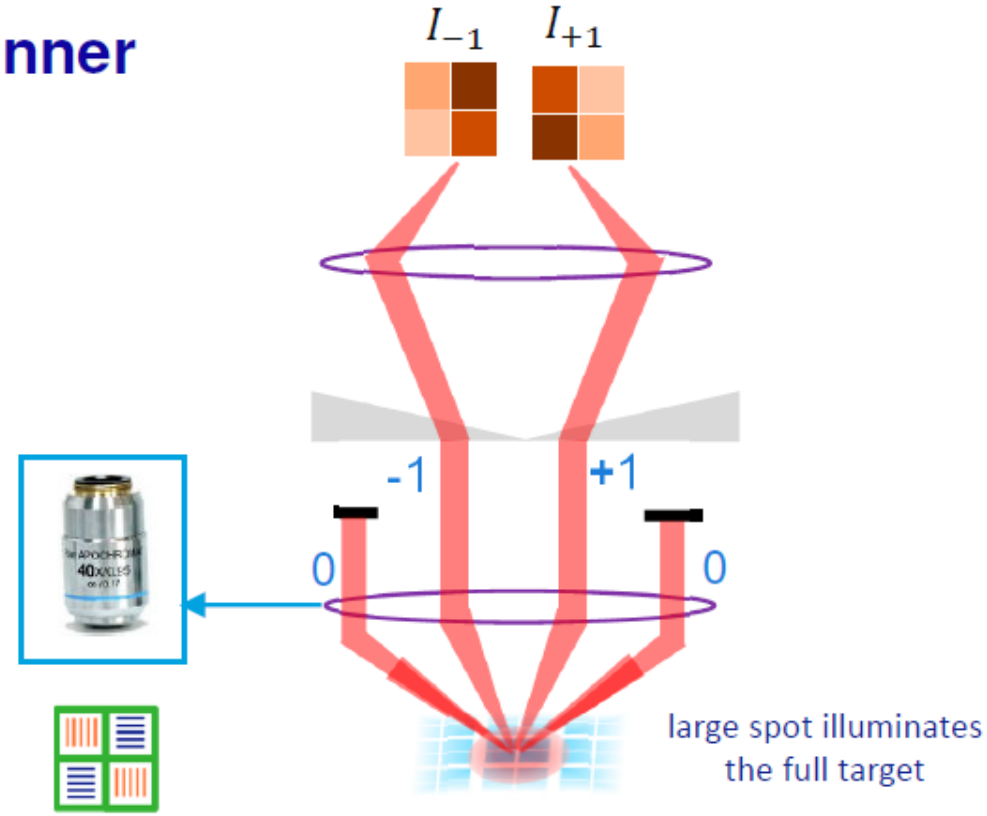


Layer thickness variations (and secondary reflections) can cause reflections from different interfaces in the stack, leading to offsets in measured height. These offsets vary with product layer variations.

Optical Metrology outside the Scanner

Yieldstar Optical Metrology

(Scatterometry sensor for Overlay Measurement, using dark field microscopy)

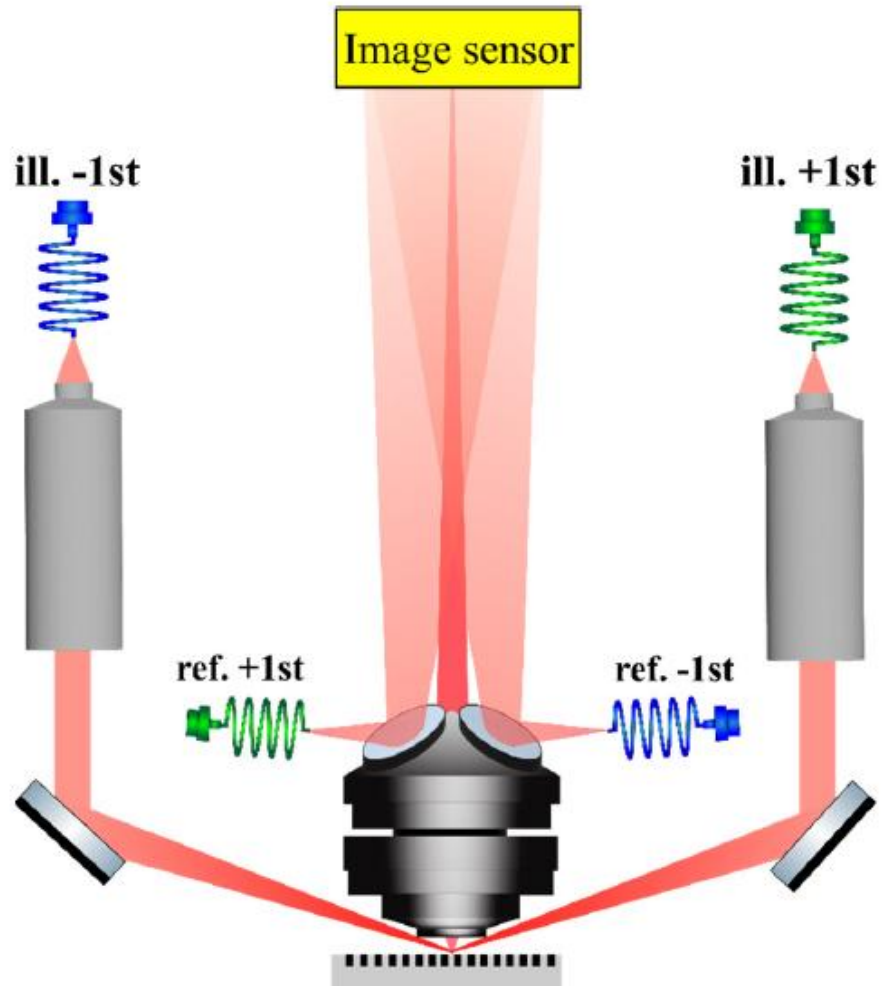


Goal:

- Overlay marks as small as possible
- With a pitch as small as possible (preferably similar to product features)
- Be robust for mark deformations
- Very fast readout (100s – 1000s marks per wafer)
- At low cost

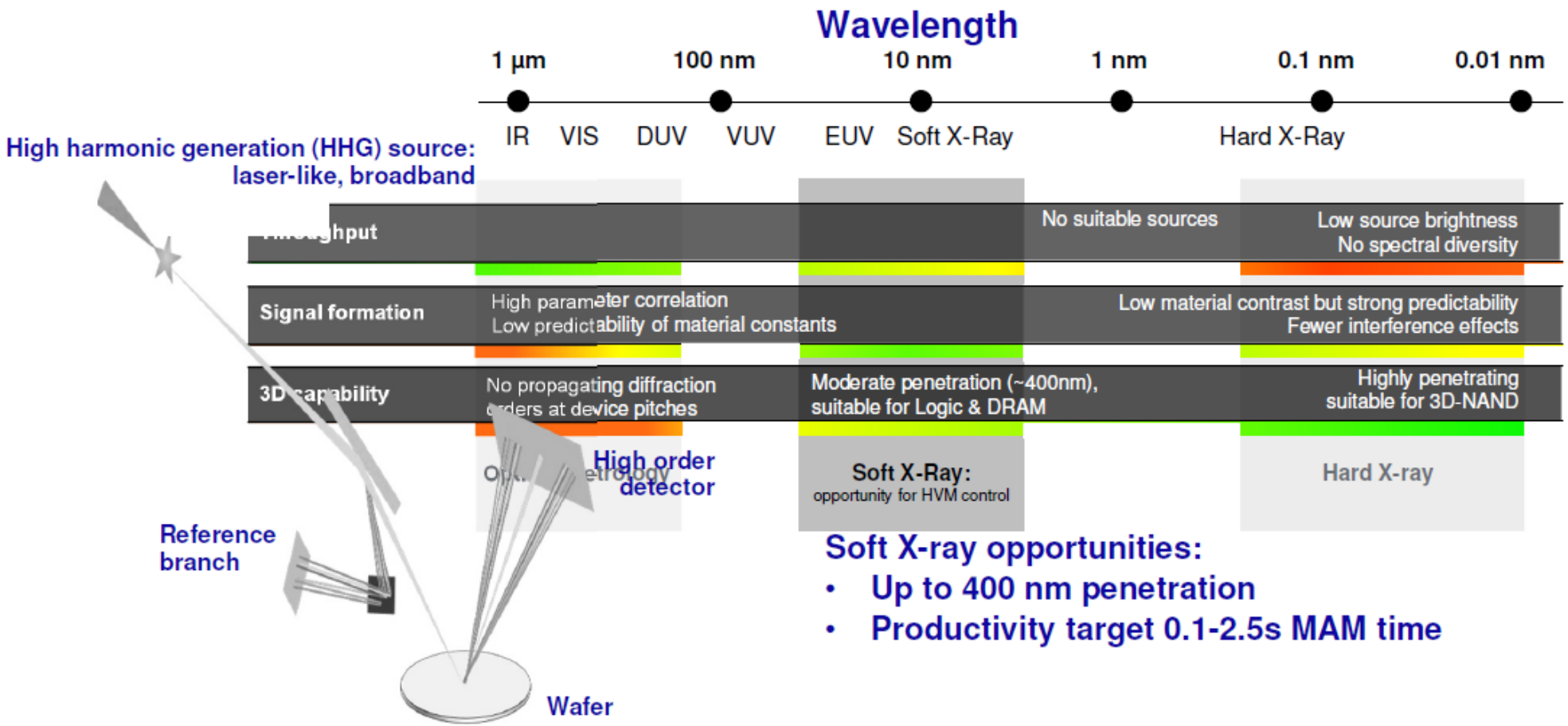
Potential Successor to Yieldstar – Digital Holographic Microscopy (DHM)

- Yieldstar optics become more complicated with each new generation
- DHM may offer a solution forward:
  - Simpler optics
  - Coherent illumination
  - Phase retrieval via digital holography
  - Strong computational correction possibilities
  - Simpler optics allow for more broadband use (towards the IR)



New 3D metrology tools needed to measure 3D structure with nm accuracy

Soft X-ray (10-20nm)



Soft X-ray opportunities:

- **Up to 400 nm penetration**
- **Productivity target 0.1-2.5s MAM time**

Innovation ecosystem from design to manufacturing

Public

ASML Research vision on academic collaborations for competence build-up

- Plan to move to broader and more strategic academic collaborations:
  - ASML relevant competences have been bundled into 7 main themes (see next slide). Target is to align 80% of academic collaborations along these 7 themes
  - Added 8th theme on technologies enabling future devices (adjacencies). Target is to align 20% of academic collaborations along this 8th theme
  - We are looking for longer term collaborations (~10 years), ensuring a build-up of knowledge and expertise in academic research groups. Research groups are encouraged to make (joined) research roadmaps, showing what they want to address in the next 10 years
  - We are looking for broader collaborations, encompassing multiple universities, RTOs, and other industrial partners (for pre-competitive research or research in different fields-of-use), building on the strength of the individual partners
  - There will always be room for short/small academic collaborations
  - We keep looking for the right funding instrument with healthy financial leverage
  - We will look to build up and secure relevant IP

- For now, we focus on Dutch universities and a small number of close-by international universities (Leuven, Antwerpen, Aachen, Lund, Heriot-Watt). → Travel distance, Funding instruments, Building up of IP position
- We will explore other non-Dutch academic partners only if they add something to the network that is not available at Dutch universities, or if they offer something that is very significantly better than the state-of-art in Dutch universities

Public

Topics identified as important for ASML

1. Optics (Integrated Optics, Free space optics, Meta-surfaces/meta-lenses, Opto-mechanics/Opto-mechatronics, Optical design, Optical coatings, Computational optics, Light sources, Cameras & Detectors)
2. Measurement/metrology (Science of measurement, Dimensional metrology, Gauge R&R)
3. (Physics based) machine learning for lithography and metrology applications (Bayesian inference, Large Language Models, Predictive maintenance and Diagnostics)
4. Electron optics (Electron sources, Electron detectors, Electron imaging, Aberration correction, Image processing)
5. Mechatronics (Superconducting actuation, Modeling & Control theory, Advanced manufacturing, Advanced design including topology optimization, Opto-mechatronics)
6. Material interaction in harsh environments (Plasma surroundings, EUV irradiation, Immersion, Tribology, Resistant material characterization/specification/design/manufacturing, Chemical contamination, Particle contamination).
7. Modeling and control of continuous media (Measurements and modeling of plasma and plasma-materials interaction, Measurement of flows and temperatures, Temperature and flow simulations (CFD), Cooling and Heating concepts, Resist modeling and Stochastics, Etch and deposition modeling).

8. Technologies enabling future devices (Etch, Deposition, Alternative materials, 2D materials, 3D integration)

Public

Public